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DESIGN OF LOW POWER AND AREA EFFICIENT SRAM ARCHITECTURE BASED ON GDI TECHNIQUE

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Abstract: Semiconductor memories are most important subsystem of modern digital systems. In new era the scaling of silicon technology has been ongoing, due to scaling large memory can be fabricated on a single chip as results memories are capable to store and retrieve large amount of information at high speed. But due to high density, power dissipation gets increases and speed decreases. So there is need for the design of low power and high speed circuit in memory. Here presents a new five transistor (5T) CMOS and Fin FET SRAM cell to accomplish improvements in stability, power dissipation, and performance over previous designs, for high speed and high stability memory operation. 5T SRAM using low power reduction techniques. All the simulations have been carried out at Tanner EDA tool. In this project, will modify 5T SRAM cell with the use of high threshold PMOS Devices that results in decrease in the leakage that reduces power dissipation. The circuit designing and simulation is done on the Tanner tool, Schematic of the SRAM cell is designed on the S-Edit and net list simulation done by using T-spice and waveforms are analyzed through the W-edit.

Keywords: 5T SRAM Cell**,** Power Dissipation, Delay, Cell area

1. Introduction

Low power design of SRAM is important role in today's vlsi technology. Static Random Access Memory (Static RAM or SRAM) is a type of RAM that holds data in a static form, that is, as long as the memory has power. The two stable states characterize 0 and 1. During read and write operations another two access transistors are used to manage the availability to a memory cell.

The total power dissipated in a typical SRAM architecture is the sum of two components.

1) Active power dissipation
2) Standby power consumption due to leakage currents of the cross coupled CMOS inverters within each cell

Future Electronics has a wide range of static RAMs from several chip manufacturers that can be used for programming a SRAM memory card or for any other devices requiring static random access memories.

With the FutureElectronics.com parametric search, when looking for the right static RAMs, you can filter the results by category. We carry the following categories of static RAMs:

- Synchronous SRAM
- Asynchronous SRAM

Asynchronous SRAM:

Independent of clock frequency; data in and data out are controlled by address transition.

Synchronous SRAM:

As computer system clocks increased, the demand for very fast SRAMs necessitated variations on the standard asynchronous fast SRAM. The result was the Synchronous SRAM (SSRAM). Synchronous SRAMs have their read or write cycles synchronized with the microprocessor clock and therefore can be used in very high-speed applications. An important application for synchronous SRAMs is cache SRAM used in PCs.

2. Existing Design

2.1 6T Sram cell operation

6T static random-access memory is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance, but is still volatile in conventional sense, that data is eventually lost when memory is not powered.

2.2 Power Dissipation

In order to calculate the average power dissipation of the cells, proper bit sequences are inserted to the bit lines to cover all the possible transactions. More specifically, the repeating sequence of transactions that each cell performs is: write 0 (writing 0 when data = 1), write 0 (writing 0 when data = 0), read (reading 0), write 1 (writing 1 when data = 0), write 1 (writing 1 when data = 1), read (reading 1).

2.3 Standby Mode (the circuit is idle)

In standby mode word line is not asserted (word line=0), so pass transistorsA1and A2 which connect 6t cell from bit lines are turned off. It means that cell cannot be accessed. The two cross coupled inverters formed byD1-D2 will continue to feed back each other as long as they are connected to the supply, and data will hold in the latch.

2.4 Read Mode (the data has been requested

In read mode word line is asserted (word line=1), Word line enables both the access transistor which will connect cell from the bit lines. Now values stored in nodes (node a and b) are transferred to the bit lines. Assume that 1 is stored at node a so bit line bar will discharge through the driver transistor (D1) and the bit line will be pull up through the Load transistors (P1) toward VDD, a logical 1. Design of SRAM cell requires read stability (do not disturb data when reading).

2.5 Write Mode (updating the contents)

Assume that the cell is originally storing a 1 and we wish to write a 0. To do this, the bit line is lowered to 0V and bit bar is raised to VDD, and cell is selected by raising the word line to VDD.

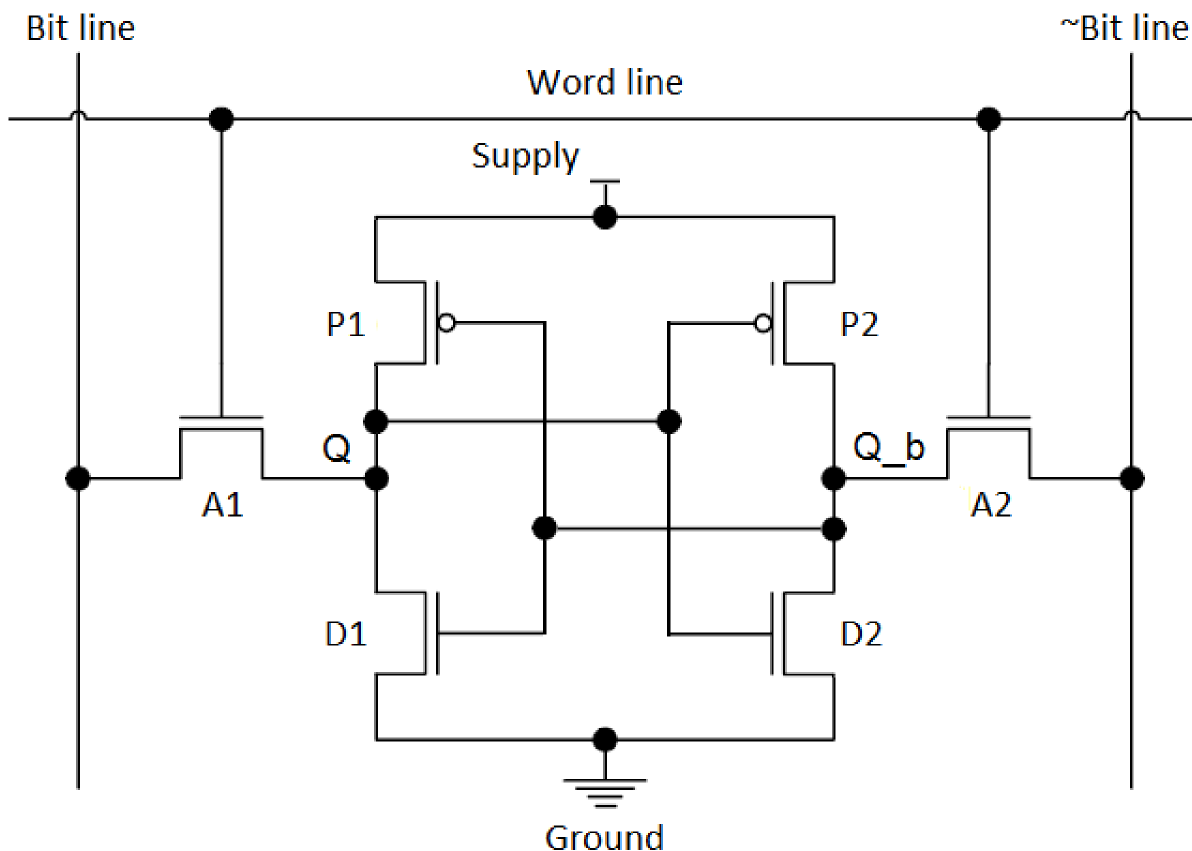


Figure: 1 Basic 6T SRAM cell

3. Modified 6t sram cell

The modified 6T cell too uses too inverters but one of the inverters is made with pseudo NMOS technology and another with CMOS technology. Pseudo NMOS logic is an advanced CMOS logic technology which has advantages like low area requirements, low gate load capacitance for input signals which helps in faster switching. The proposed modified 6T cell is shown in Figure3.5 which produces low power dissipation.

SRAM cell uses two inputs lines namely WL (word line) and BL (bit line). Write lineacts like an enable pin which is connected to gates of the transistors 1 and 2. BL represents the bit that needs to be stored and BLB its complement. To perform write operation, we need to keep the BL line in the required state by keeping the WL pin in low state and then change the state of WL pin to high. The two inverter circuits connected to each other are responsible for holding the data. To perform read operation, we need to make BL and BLB high. After this, either of the BL and BLB lines will be pulled low because it gets discharged due to the zero state present on one of the inverters. The cell occupies less area but when it comes to data stability, difficulties arise. This data instability is the result of high noise margin.

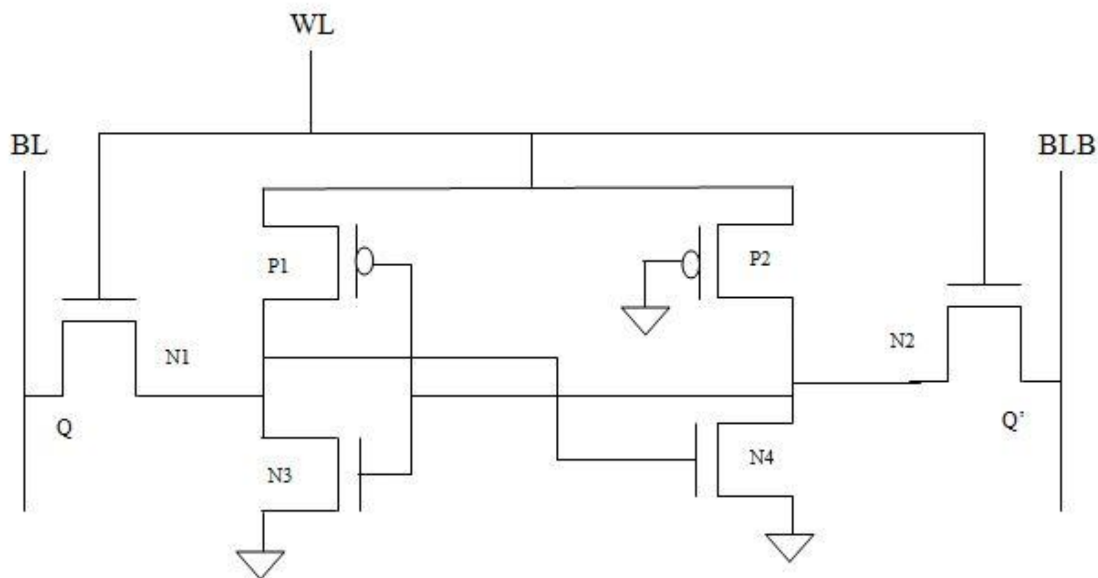


Figure: 2 Modified 6T SRAM Cell

4. Proposed Design

A five-transistor SRAM intended for the advanced microprocessor cache market. The goal is to reduce the area of the cache memory array while maintaining competitive performance. Various existing technologies are briefly discussed with their strengths and weaknesses. The design metrics for the five-transistor cell design, performance and stability are to be evaluated. Finally a comparison is done between an existing six transistor technology and the proposed technology. The comparisons include area, delay and power.Fig. 3 shows the proposed five transistor (5T) SRAM cell. In this cell, Inverter NMOS transistors (M1, M3)

are directly connected to the bit lines, PMOS transistors (M2, M4) are connected to power supply voltage (VCC), and there is an additional transistor M5 coupling the inverters. Unlike standard cell, no word line transistors are needed to provide access during the read and write cycles.

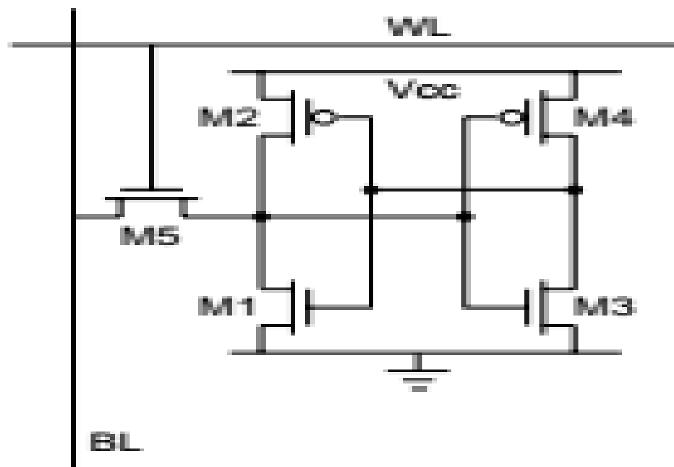


Figure: 3 5T SRAM Cell

5. Gate diffusion input

Vlsi technology has developed over the years there by enhancing the performance of chips in terms of three basic constraints delay,power and area.Gate Diffusion Input Technique is one such method which attempts to minimize the delay and power consumed by the circuit.

5.1 Basic GDI cell

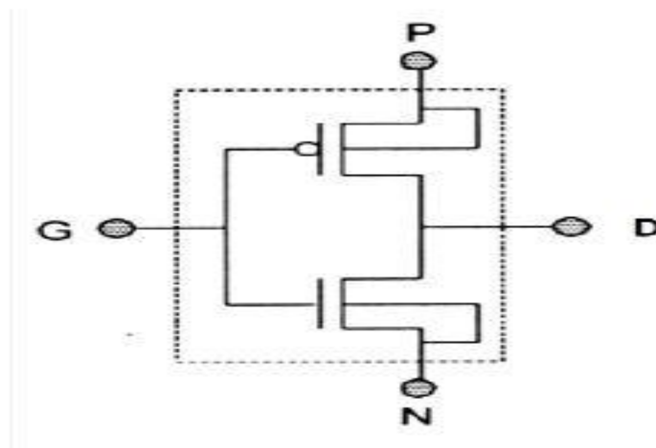


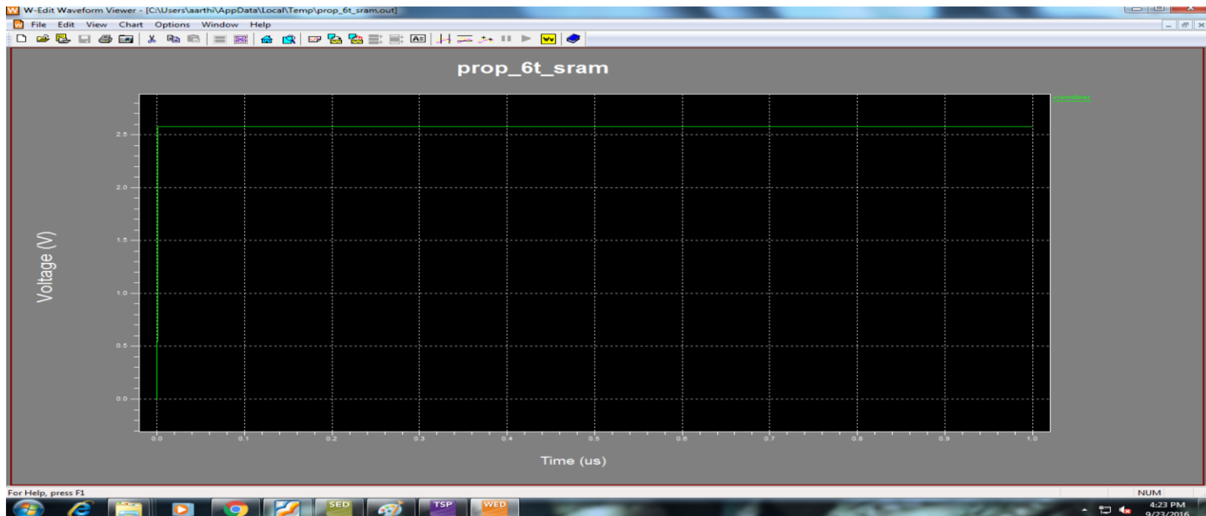
Figure: 4 Basic GDI Cell

The GDI method is based on the use of a simple cell as shown in Fig.4 At a first glance the basic cell resembles the standard CMOS inverter, but there are some important differences GDI cell contains three inputs – G (the common gate input of the NMOS and

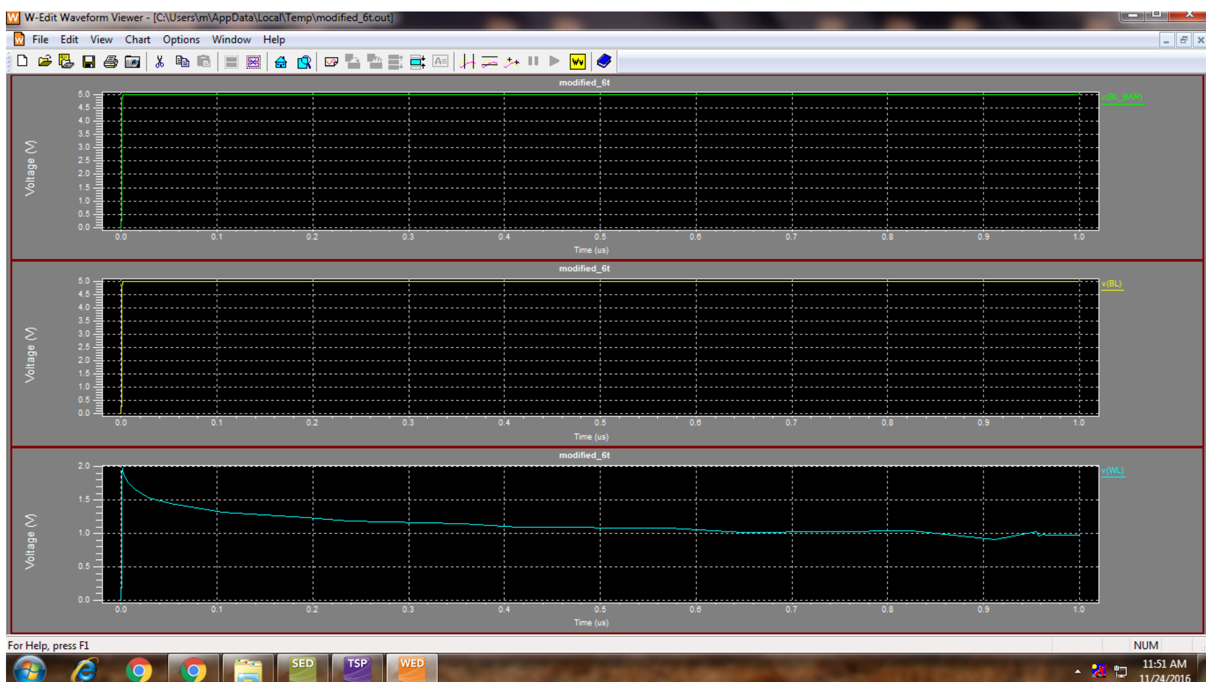
PMOS transistors), P (input to the outer diffusion node of the PMOS transistor) and N (input to the outer diffusion node of the PMOS transistor).

6. Results and Discussion

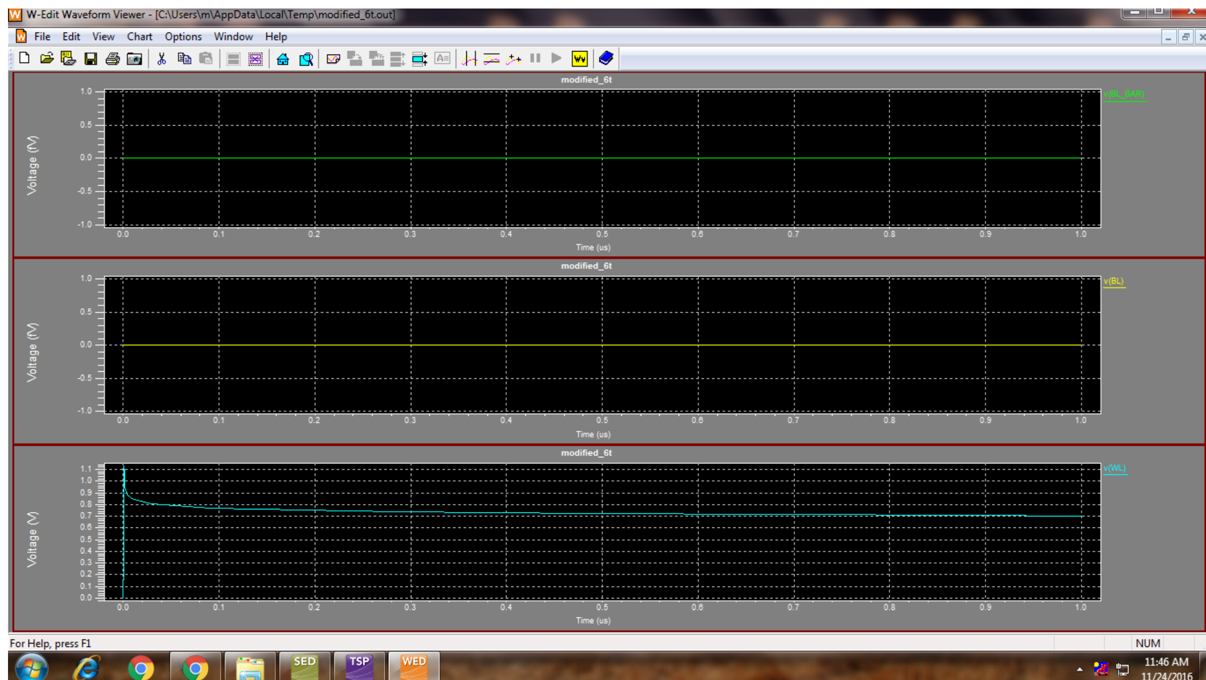
6.1 6T sram output waveform



6.2 Modified 6T sram read operation output waveform



6.3 Modified 6T sram write operation output waveform



7. Conclusion

The proposed 5T SRAM cell design would be suitable for various high speed and low power embedded cache. 5T SRAM cell performs the write operation using a single bit line to reduce the dynamic power consumption. The proposed SRAM cell is suitable for real time video applications. The 5T cell is attractive for high performance arrays. It also provides tolerance when compared to existing method. This eliminates the need for secondary or dynamic power supplies and enables low voltage operation. Simulation and analyzes the performance of 6T SRAM cells, its reduces power consumption, delay and number of transistors. Read and write operation was done using the 5T SRAM method.

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