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Design of Finite Impulse Response Filter Architecture using Wallace Tree Multipliers

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Abstract

Finite impulse response (FIR) filter is one of the main key mechanisms in any communication systems. The output of the system is relates to the FIR filter, so need to design an efficient FIR filter, to get a perfect output. Filter design contains many blocks; one of the main blocks is multiplier. Many types of multipliers are available in the digital circuits, but need an efficient multiplier design to get better filters. Multiplier is one of the basic building blocks in the digital circuits. So the performance of the multiplier is important to get an efficient circuit design. Power consumption is one of the major drawbacks in the multiplier. Power consumed by the multiplier is higher in the digital circuits. Wallace tree multiplier was designed and implemented using verilogHDL. This multiplier reduces the stages of partial product addition. So this multiplier takes less number of gates to implement and also it overcomes the existing multiplier drawbacks. Finally the designed multipliers are applied into the FIR filter, and show the best filter.

Keywords: Low power multiplier, Reversible Logic gates, Digital circuits, Verilog HDL

I. Introduction

Finite-impulse response (FIR) filters take part in an important role in many communication systems. Wide range of responsibilities such as noise cancellation, harmonized filtering, nosiness cancellation, attenuation reduction, channel equalization, etc. Different types of architectures and execution method were planned to develop the performance of filters. The unstoppable growth in multimedia and mobile applications has enlarging the require for low power digital signal processing and Wireless Communication. One of the mainly used functions executed in digital signal processing is Finite Impulse Response (FIR) filtering. FIR filter structures are simplified to minimizing the number of operation like additions, subtractions, shifting; multiplication. In FIR filter order varies the stop band energy of the input signal. Reconfigurable FIR filter structural designs were done for low power applications. Multiplications are important operation in FIR filters. But the weight of the filter is constants. Some techniques were developed over the years for the efficient realization of constant

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multiplications by a network of add and subtract, shift operations. Constant multiplication methods are classified into two types first is single constant multiplication (SCM) methods and second one is multiple constant multiplication (MCM) methods.

Single constant multiplication methods are useful to multiply a variable operand with a well-known constant, where the multiplications are realized by a number of add, sub and shift operations accompanied by shifting operation. Multiple constant multiplication methods are applied for multiplication of one variable operand with number of constants, the intermediate results can be shared across the entire network to minimize the overall computational complexity.

II. Related Works

J. Chen, and W. Ding [1] have been proposed the concept of FIR Filter with low power based on multipliers and adders. This proposed method includes low power multiplier, RCA adder, modified booth multiplier, and shift and add multipliers, breakdown transformation in architecture of linear phase and applied to filters for consumption of power. A. Dandapat et al. [2] was presented concept architecture of high performance FIR filter for static and reconfigurable applications. Transpose structure of FIR filters are pipelined and support MCM technique.

V. Gowrishankar et al [3] have been proposed FIR filter with reconfiguration based architecture to deal the Filter Performance for changing the Power Consumption. When the filter order is set and not changed for exacting applications, and filter performance can be made using the proposed architecture. The power savings is up to 40.3% with minor degradation, and the area overhead of the proposed scheme is less than 4.9%. T. Hentschel et al. [4] presented a novel concept of area and power efficient digital FIR Filter design using modified MAC unit. The design of digital finite impulse response (FIR) filter for digital signal processing (DSP) in this project shows Power Delay Product (PDP) is improved by 16.80% and 12.54%.

Jagadeshwar Rao et al [5] explained a design of unsigned 32-bit multiplier. This architecture consists of a modified Radix-4 Booth encoder, a modified Wallace tree adder and a carry look ahead adder. The altered Wallace tree adder sums all the partial products with their complement carry to find the final multiplier. It is done by dividing the summing process into three computation areas: signed area, MSB area and LSB area. The signed area is computed separately with MSB and LSB areas computation. In the MSB and LSB areas computation. Kumar et al [6-7] a parallel architecture was designed to find the optimum delay.

III. Wallace Tree Multiplier Design

Array multiplication is performed by using Wallace tree multiplier Wallace multiplication is also knows as parallel multiplier. Array multiplier occupies more number of

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gates to perform multiplication operation. It occupies large area for computation. To overcome this problem, Wallace multiplier is designed; the multiplier design was done by using proposed SQRT CSLA. To improve the speed by modify the Carry select adder using D-Latch in the place of BEC. The existing square root carry select adder having RCA and BEC, whereas RCA or D Latch was used in previous architectures. The Conventional Group2, Group3 and Group4 structures contain FA, HA, BEC Converter and MUX circuits. Usual Square root select adder offers high speed and less delay than the earlier structures.

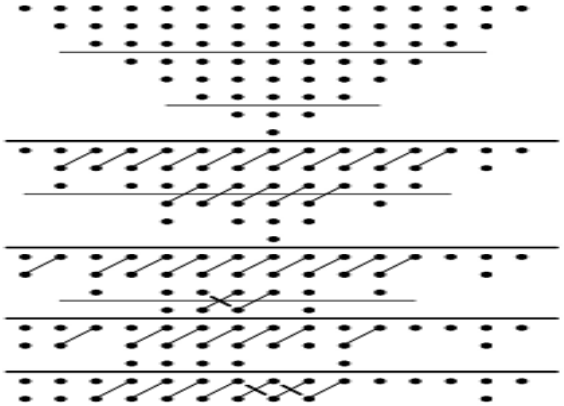

Fig. 1 Structure of reduced complexity Wallace tree multiplier

Fig.1 shows reduced complexity Wallace multiplier structure. The Wallace multiplier consists of reduced number of HA (half adder), FA (full adder) when compared to the usual Wallace tree multiplier. In the modified circuit, AND gates in the partial products are arranged in an inverted triangle order. The operation is separated into three row groups in the reduced complexity Wallace multiplier. FA is used for adding three bits.

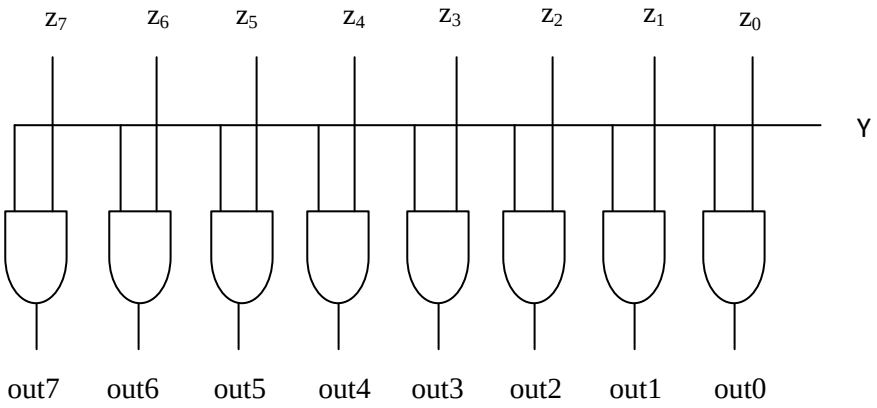

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Fig. 2 Partial Products generation stage of Wallace tree multiplier

IV. Proposed FIR Filter Structure

Finite Impulse Response (FIR) filter is used to filter the noise, attenuation and unwanted signals at finite impulse durations. Multiplication and Accumulation (MAC) unit predicts the duration of periodic impulses response. High performance of multiplication and accumulation unit architectures is required to improve the performance of the entire digital FIR filter. SQRT CSLA based Wallace tree multiplier is implemented into the multiplication of direct form FIR filter. So we can improve the performance of digital FIR filter than other existing FIR filters. The performance is analyzed by using the simulation environments.

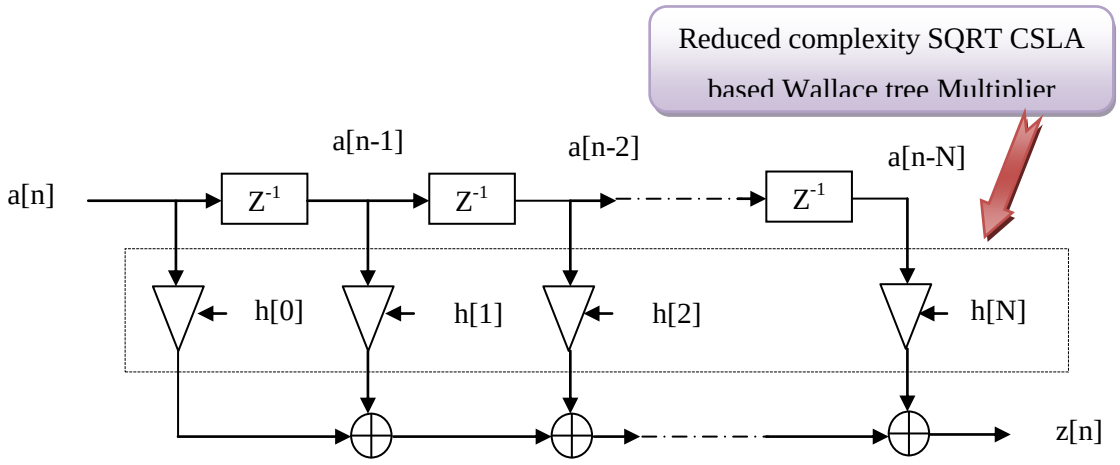

Fig. 3 Structure of Direct Form FIR Filter

In fig.3 shows the direct form FIR filter structure, the figure clearly explain the operation of FIR filter. Output of the filter based on the number of order used in the filter structure. Each order of the filter using one multiplier. Based on the multiplier operation the performance of the filter is achieved. Here using the Wallace tree multiplier for multiplication operation. This multiplier produced the better results during the filtering operation.

V. Simulation Results

Simulation was done by using the ModelSim XE III 6.3c simulator. Parameters like area delay and power can be analyzed by using Xilinx ISE 10.1 simulator. Output of the Vedic multiplier is same as other multiplier, compared to the other multiplier speed and accuracy of the Vedic multiplier is higher. The result is shown in the figure. 4 contains different combination of inputs, based on the input it produced the output.

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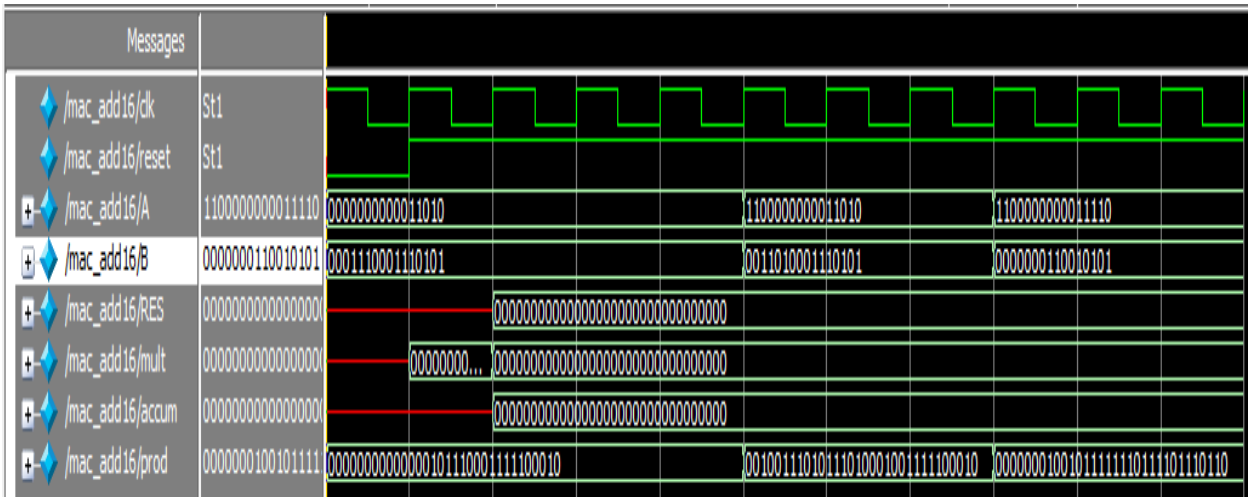

Fig. 4 Simulation Output of Wallace tree Multiplier

VI. Performance Evaluation and Comparison

Table No.1 Comparison of Area and Delay between Existing and Proposed system

Parameters	Conventional Multiplier	Proposed Wallace tree Multiplier
LUTs	149	120
Slices	98	75
Delay(ns)	20.440ns	19.164ns
Power(mW)	874mW	736mW

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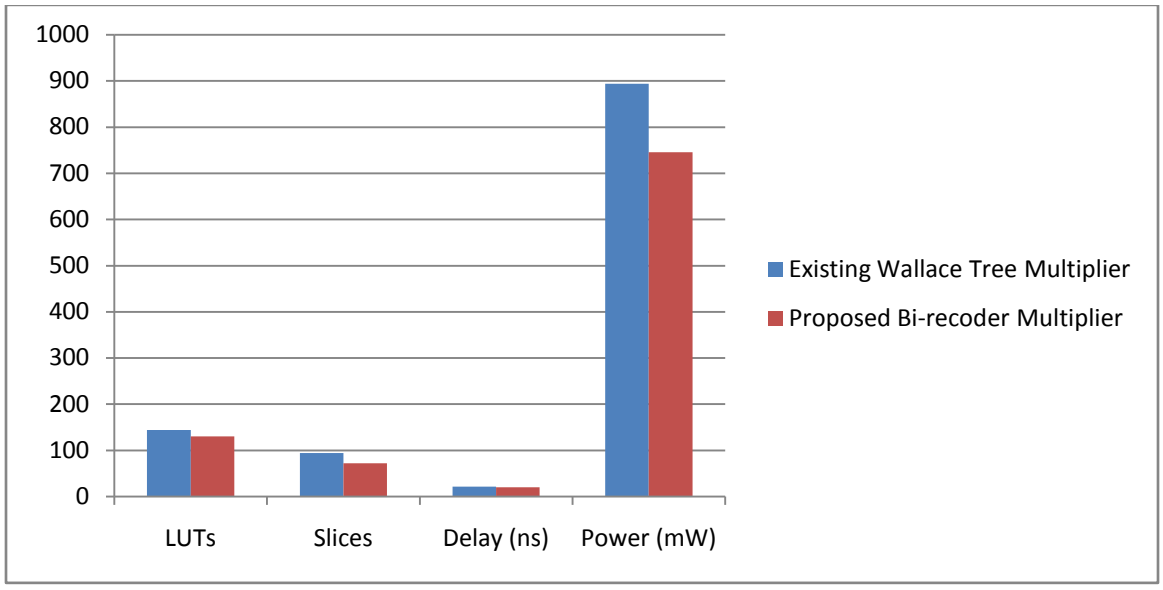

Fig. 5 Graphical representations of Area, Delay and power

In fig.7 shows the difference in existing and proposed multiplier design. It is clearly explain the parameters are reduced when compared to the previous multiplier design.

VII. Conclusion

An area efficient and high speed multiplier Wallace tree multiplier was designed. It reduces the area complexity, latency and high power dissipation in the digital circuits. The proposed multiplier was applied to the direct form FIR filter for verifying the filter operation. After applying the multiplier into the filter, the performance is evaluated. The proposed Wallace tree multiplier based FIR filter offers 19.4% reduction LUTs, 23.4% reduction in slices, 6.2% reduction in delay and 15.7% reduction in power. It provides the improved results when compared to the other FIR filters. Now the filter is applicable for much application like digital signal processing, wireless communication, image processing etc. The modified FIR filter is suitable for all kind of applications.

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