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LOW POWER 128 POINT SPLIT RADIX FFT FOR LTE APPLICATION

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Abstract - In this paper, we describe a processor architecture customized to Split radix FFT algorithm. The proposed architecture supports all FFT sizes, required by the LTE applications. The proposed design is aimed to reduce the area, latency, power and also to reduce the number of computational path in order to speed up FFT processor computation. The proposed low power 128 point split radix FFT architecture applies various periodicity properties of twiddle factors multiplier.We implement the processor in 128-point MDC architecture with split radix algorithm. The processor has been synthesized on a Xilinx ISE 10.1design technology and both energy-efficiency and performance have been evaluated.

Keywords - Fast Fourier Transform, Long-Term Evolution, Multipath Delay Commutator (MDC) FFT.

1. Introduction

Wireless data transmission techniques face a lot of challenges in the present world. Based on improving their architecture exploration, different LTE model has been designed by great endeavours. The various types of sources such as digital bits, voices, videos, full broadcast messaging, command and control signals are considered to realize the data transmission properties of OFDM system. Orthogonal Frequency Division Multiplexing (OFDM), Software Defined Radio (SDR) and Long Term Evolution (LTE) technology bring cost efficiency, flexibility, and power consumption to drive and establish long distance communications.

Traditionally, it is not possible to transmit timing signal over a long distance. Thus it is required to design the conversion process of timing signal into the frequency signal. Fast Fourier Transformation (FFT) technique is one of the important frequency transformation techniques in which twiddle factor multiplication performs the conversion process. Twiddle factor is also referred to as the rotational factor. In twiddle factor multiplication, the frequency response of corresponding timing signal should be found with the help of amplitude and phase shift of the corresponding signal.

In LTE, calculation of DFTs of a series of OFDM symbols is required with the speed of 66.67 μs per symbol. Each symbol is a vector of complex numbers of the length N, where N = 128, 256, 512, 1024, 1536.Split-radix FFT architectures are proposed as an alternative to radix-2 and radix- 4 FFT architectures. The emerging communication standard, LTE (Long Term Evolution) requires 128-2048/1536 size FFT, providing a flexible spectrum support from 1.4 up to 20 MHz. In LTE systems, information are transmitted in resource blocks each containing

subcarriers. The number of resource blocks can be increased and distributed in both time and frequency when needed. Using OFDM (Orthogonal Frequency Division Multiplexing), the occupied subcarriers will hence vary over time, according to the current transmission bandwidth and the allocated resource blocks.

The proposed design should be extremely low-power and low-cost to be useful, since, the main aim of the devices are portable consumer electronics such as mobile phones, laptops, etc. On the other hand, business models require flexible programmable implementations. An important use case is SDR where software implementation of several radios, one of them typically being LTE, should be supported on top of a shared hardware platform.

In this work, we propose a new customized 128-point FFT architecture based processor for FPGA implementation of split-radix FFT. In particular, FFTs of all the sizes required in LTE, 128, 256, 512, 1024, 1536, and 2048, are supported. Compared to the results of proposed architecture achieves not only higher flexibility, but also achieves better performance obtained by the optimization of the previous designs.

2. Literature Survey

Pipeline based split-radix FFT architecture has been developed [1] for improving the combinational and sequential delay. This article presents a full custom one-bit slice delay commutator design for pipeline split-radix FFT (SRFFT) architecture. Pipelining register is added in every input/output block in the proposed FFT structure. Pipelined architecture has AND gated D Flip-flop (DFF). It reduces the sequential delay before clock and after the clock. Butterfly Unit (BU) or Processing Element (PE) architectures are explained briefly in this article.

New area efficient and power efficient 128-point FFT processor has been designed for practical Ultra-Wideband (UWB) applications [2]. To develop and execute a 128-point FFT, the non-Cooley-Tukey radix-8 unit can be developed and implemented in this research work. Complementary Metal Oxide Semiconductor (CMOS) – 0.18um technology has been used to establish a 128-point FFT algorithm. The proposed architecture of this research work can be saved by 20% to 63% approximately when compared to R2SDF FFT architecture. The measurement result of this work shows the throughput rate is 409.6Msample/s at the working frequency of 132MHz. These specifications can meet the specification of the UWB system; hence radix-8 butterfly structure based frequency transformation technique will be helpful in UWB system.

Requirements for the LTE system contain improved system capacity and coverage, improved user experience through higher data rates and reduced latency, reduced deployment and operating costs and seamless integration in [3]. They developed an EDEM unit which supports the 25, 16, 9, 8, 5, 4, 3 and 2-point FFT. The EDEM improve the throughput rate 2x~4x than the state of art technology for the applying of high radix factorization. The EDEM is used for reducing hardware complexity. The speed-area factor of proposed FFT processor is three times than Xilinx IP core and nearly two times than GMR in [4].

Adaptive OFDM system has been implemented [5] by using FPGA. 64-QAM and 32-QAM modulation techniques have been considered in an adaptive OFDM design. Very high-speed integration circuit Hardware Description Language (VHDL) is utilized in this work to implement the modulation techniques and OFDM transmission system technologies. The best value of Signal to Noise Ratio (SNR) is considered in this work as 60dB. Hence, 64-QAM modulation based OFDM system offers the best performance than 32-QAM modulation based OFDM system. In 64-QAM modulation based OFDM system design, high speed is achieved than 32-QAM modulation based OFDM system. In proposed technique, R2SDF FFT requires 11 complex multipliers to implement 8192-point FFT, and R22SDF FFT requires 6 number of a complex multiplier to implement 8192-point FFT, and R23SDF FFT requires 4 number of a complex multiplier to perform 8192-point FFT.

3. Split Radix-FFT

In 1984, the split-radix algorithm was clearly explained and named by Duhamel and Hollman in 1984, it required smaller number total multiply and add operations operations than any past power-of-two algorithm. The split-radix algorithm can be derived by careful examination of the radix-2 and radix-4 .While in most places the radix-4 algorithm has less nontrivial twiddle factors, in most of the places radix-2 actually lacks twiddle factors present in the radix-4 structure or those twiddle factors simplify to multiplication by −i, which actually needs only additions.

$$X(k) = \sum_{n=0}^{\frac{N}{2}-1} x(2n)e^{-\left(i\frac{2\pi\times(2n)k}{N}\right)} + \sum_{n=0}^{\frac{N}{4}-1} x(4n+1)e^{-\left(i\frac{2\pi(4n+1)k}{N}\right)} + \sum_{n=0}^{\frac{N}{4}-1} x(4n+3)e^{-\left(i\frac{2\pi(4n+3)k}{N}\right)}$$

$$= \mathrm{DFT}_{\frac{N}{2}}\left[x(2n)\right] + W_N^k \mathrm{DFT}_{\frac{N}{4}}\left(x(4n+1)\right) + W_N^{3k}\mathrm{DFT}_{\frac{N}{4}}\left(x(4n+3)\right)$$

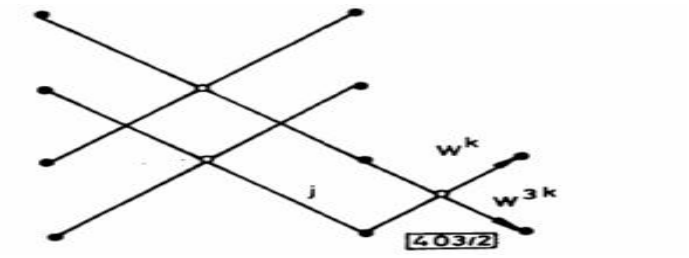

Fig 1.Split radix FFT structure

4. Multipath Delay Commutator FFT

MDC FFT algorithm is based on pipelining technique. It is also referred as "stream-like" processing of block based algorithm. In order to reduce the required chip size of FFT computation, more number of delay elements is inserted in MDC FFT. Therefore, more number of independent blocks can be processed in a parallel manner. Due to more number of delay elements, speed of MDC is comparatively low. However, the chip size and power consumption of MDC FFT can be improved significantly. The structure of 8-point MDC FFT is illustrated in fig. 2. In MDC FFT structure, input sequence is broken into two parallel data streams flowing forward with correct "distance" between data elements entering the butterfly scheduled by proper delays. Both multipliers and butterflies are less utilization in MDC FFT structures. In fig. 2, C2 represents the commutator structure and BF2 represents the butterfly structure.

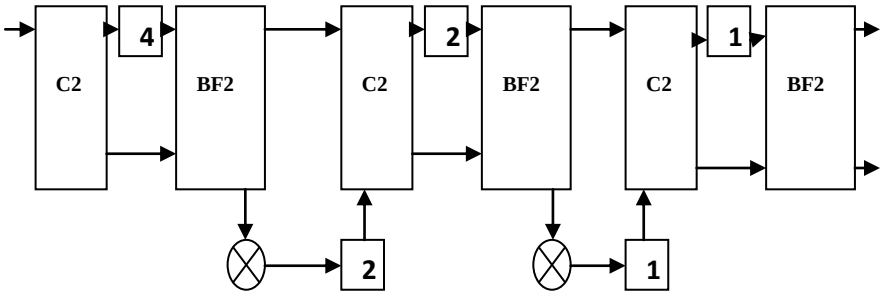

Fig. 2 Multi-path Delay Commutator (R2MDC) FFT

One of the straightforward approaches for pipeline implementation of R2MDC FFT algorithm is as follows:

1. The input data sequence is broken into two parallel data streams.
2. At each stage of this architecture half of the dataflow is delayed via the memory (Reg) and processed with the second half data stream.
3. The delay for each stage is 4, 2, and 1 respectively. The total number of delay elements is 4 + 2 + 2 +1 +1 = 10.
4. In MDC architecture, both Butterflies (BF) and multipliers are idle half the time waiting for the new inputs. The 16-point MDC FFT/IFFT processor requires one multiplier, three radix- 2 butterflies and 3 commutators.

5. Proposed 128-point Split Radix FFT for LTE Application

In this paper, 64-point Split Radix Multi-path Delay Commutator FFT has been proposed. Split radix FFT is preferred to reduce the slices and LUTs and also improve the speed of FFT processor. The advantages of MDC are less hardware slice utilization and lower power consumption and disadvantage is high speed. We identified the problem of different kinds of architecture and designed a new MDC architecture.The proposed 128-point split radix MDC FFT has fewer counts of adder and multiplication than the traditional 64-point mixed–radix FFT algorithm. In the existing method, 64-point mixed radix SDF-MDC FFT has been designed.

Mixed Radix FFT is a special type of architecture. The different stages of FFT are operated by using different radix stages, so that numbers of stages are reduced and also minimizes the computation cost and number of complex multiplication. But, the data buffers become too complex and also it requires more program memory. In order to overcome this problem, split radix MDC FFT has been proposed in this paper. Split radix FFT, which is used to improve the performance of architecture and also reduce the slices and LUTs than the mixed radix FFT. Split radix FFT is different from the mixed radix algorithm. The proposed 128-point split radix MDC architecture is shown in fig3.

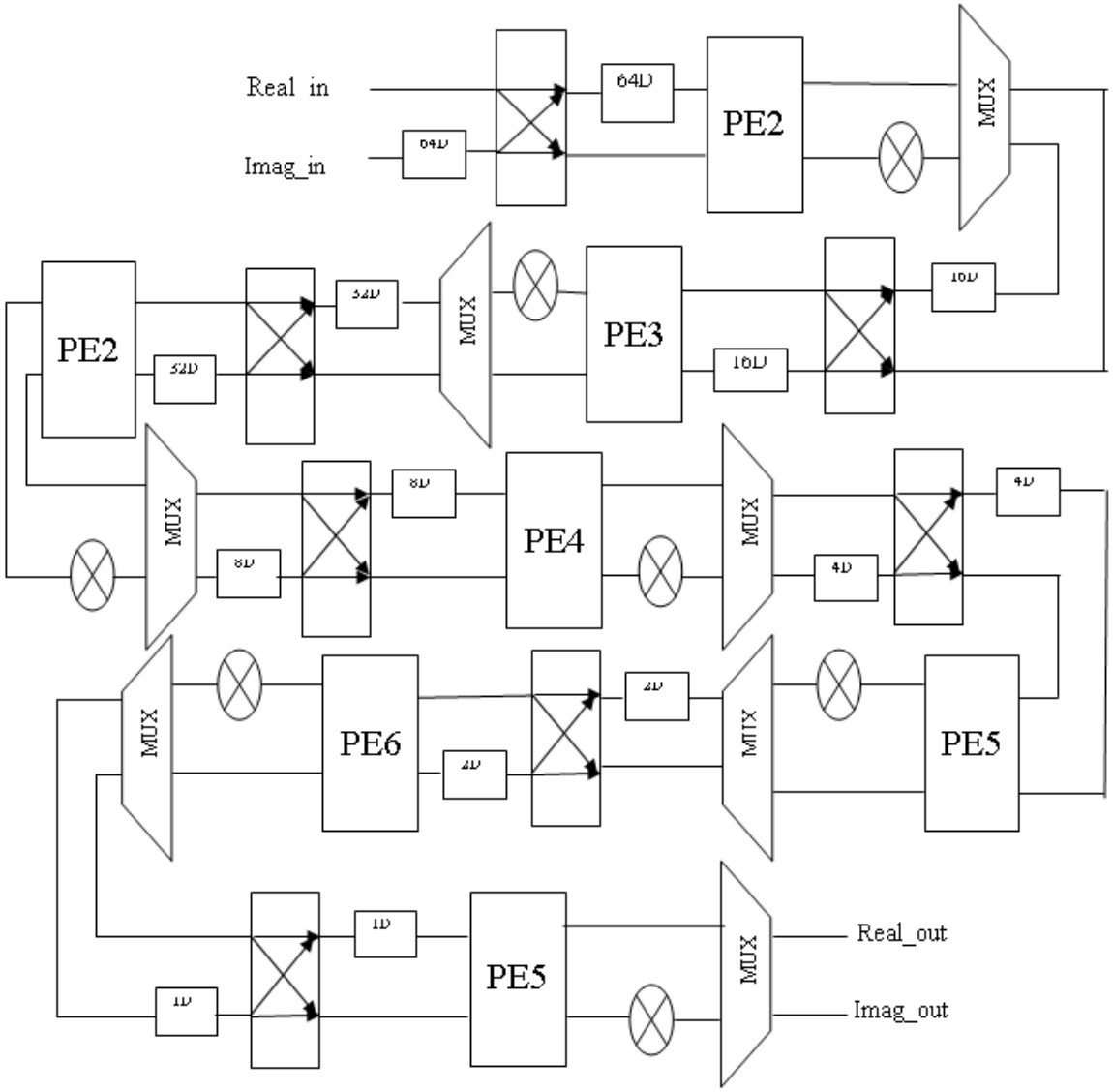

Fig 3.proposed 128-point split radix MDC architecture

These architecture consists of Processing Element (PE), Commutator, twiddle factor and multiplexer. The operation of addition and subtraction has been done in processing element. The

Commutator, which is used to convert one form of signal to another form of signal. Twiddle factor, which is used to reduce the shifter and adder values. Multiplexer is used to control the signals. Compared to traditional 64-point mixed radix FFT, the proposed split radix 128-point MDC FFT, which reduces the slices and LUTs and also improves the performance of architecture. The proposed method gives the better performance than the traditional method.

6. Results and Discussion

The proposed low power 128-point split radix FFT has been evaluated in terms of clock cycles. The proposed 128-point split radix MDC FFT has been designed by using veriog hardware description language..The design has been simulated by using 'Mentor Graphics' ModelSim simulator and the synthesis tool has been evaluated by using Xilinx Plan ahead 12.4i design tool. The simulation result of traditional 64 point mixed radix FFT and proposed 128-point split radix MDC FFT is illustrated in fig .4 and fig.5.

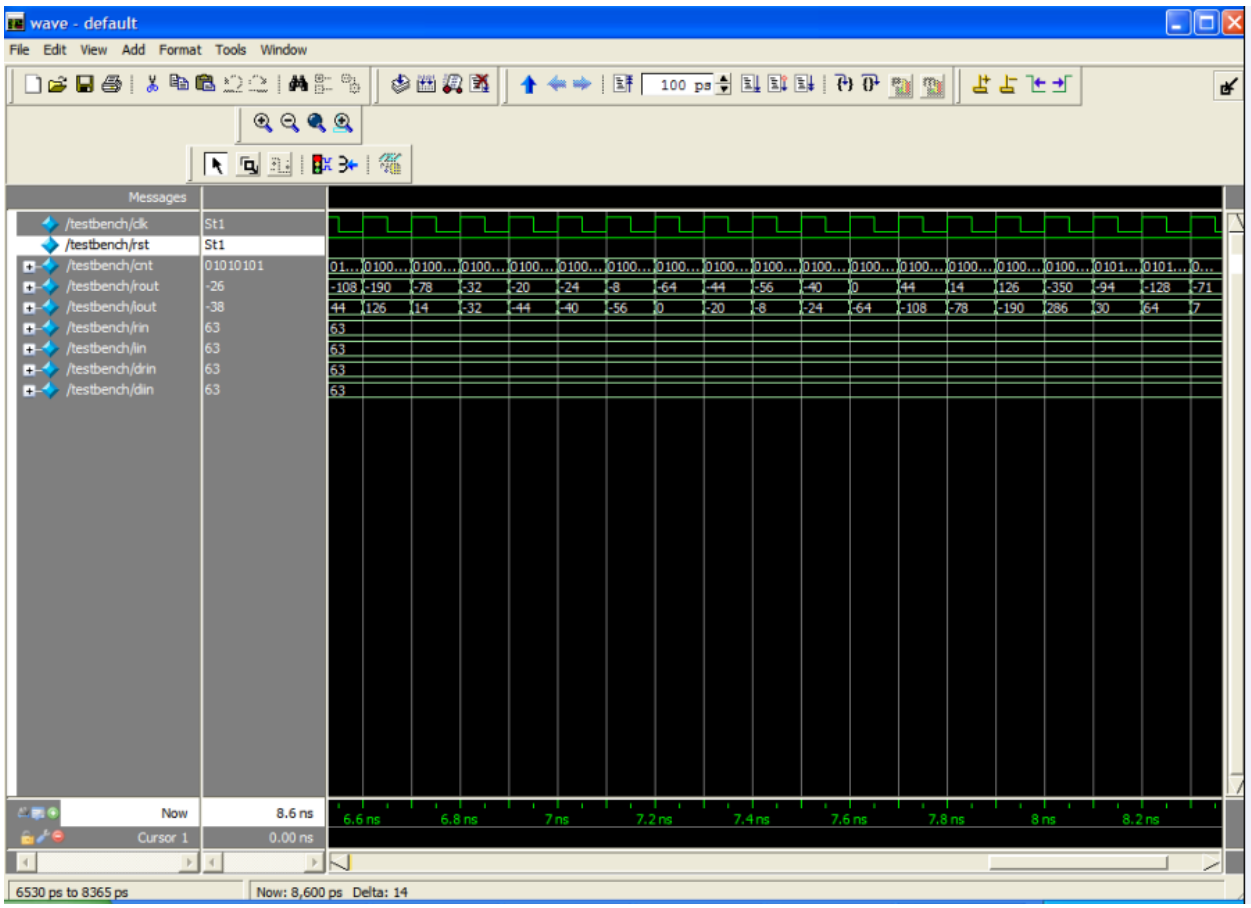

Fig.4 Simulation result of traditional 64-point mixed radix FFT

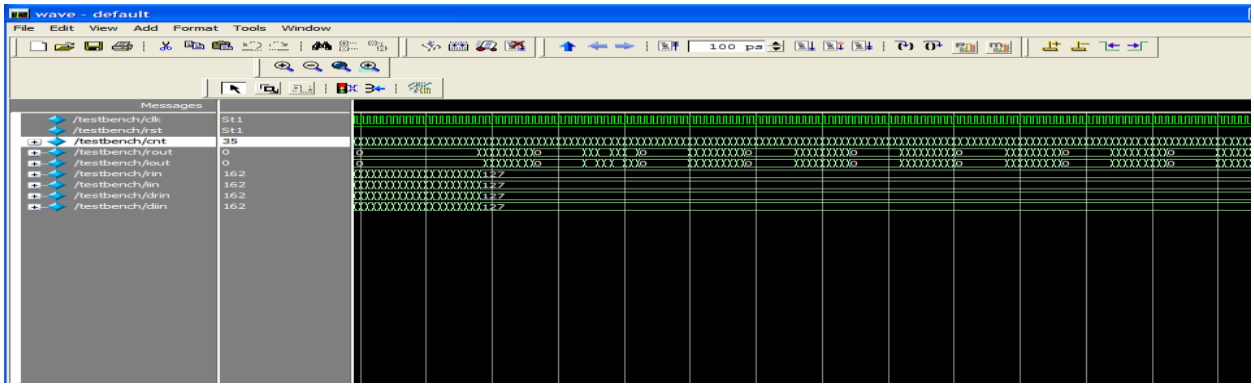

Fig.5 Simulation result of proposed 128-point split radix MDC FFT

Table .1 Comparison of traditional 64-point mixed radix FFT and proposed 128-point split radix MDC FFT

Types of parameters	Existing method	Proposed method	Percentage reduction%
Number of slice registers	7298	4,813	**34.05%**
Number used as flip flops	3733	1,692	**54.67%**
Number of slice LUTs	44,712	33,670	**24.69%**
Number used as logic	43,681	33,078	**24.27%**
Number of occupied Slices	11,311	9,408	**16.82%**
Number with unused flip flops	37,570	29,036	**22.71%**
Number of fully used LUT-Flip Flop pairs	7,142	4,634	**35.11%**
Minimum period (ns)	85.585	34.020	**60.25%**
Minimum input arrival time before clock (ns)	60.546	33.730	**44.29%**

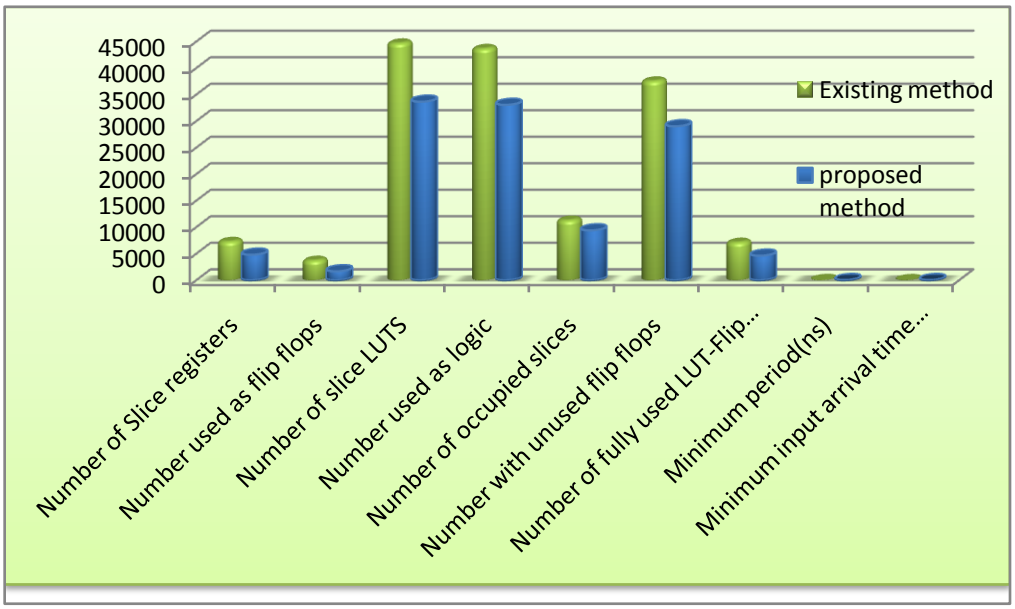

Fig.6 Performance evaluation of proposed 64-point split radix SDF-MDC FFT

7. Conclusion

Developed Multi-path delay Commutator architecture split radix FFT algorithm for LTE application has been designed. The proposed architecture has been designed through Very Large Scale Integration (VLSI) system design environment. The main aim of this research work is to improve the hardware slices, memories, LUTs and power consumption of proposed 128 point split radix MDC FFT. The number of adders and subtractors are reduced in this architecture. These proposed architecture is named as "128-point Split-Radix Multi-path Delay Commutator (SRFFT) FFT. Proposed 64-point split radix SDF-MDC FFT offers 16.82% reduction in slices, 34.05% reduction in slice registers, 54.67% reduction in flipflops, and 24.69% reduction in slice LUTs, 24.27% reduction in logic, 22.71% reduction in unused flipflops, 35.11% reduction LUT-flipflop pairs, and 60.25% reduction delay than the traditional 64-point mixed radix FFT. In future, the proposed 128-point split radix multipath delay commutator (SRMDC) FFT will be extended to large number of FFT computations for LTE –Advanced.

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