ANALYSIS OF FREQUENCY RESPONSE OF RLC NETWORKS ON SINUSOIDS OF RADIO FREQUENCIES LEADING TO TRANSMISSION LINE EFFECTS ON ROUTING NETS IN VERY LARGE SCALE INTEGRATION DEEP-SUBMICRON CIRCUITS

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Abstract - VLSI Technology has advanced to the level of transistors fabricated with gate lengths in tens of nanometers. Deep-Submicron VLSI chips need to undergo rigorous post layout simulation tests to ensure the circuit operates as expected even after fabrication. The rules for Layout vs Schematic check is also stringent for such integrated circuits. Chips operating on RF signals have Transmission Line effect along routing wires that leads to additional delays. The nets that behave as transmission lines should also be properly matched. Improper matching leads to power reflection and wastage which is not desirable in portable applications. In this work an analysis is done on nets modeled as Transmission Lines. The behavior of the transmission lines on a range of frequencies is reported in terms of amplitude response and phase response. The behavior of a transmission line depends on the geometry. Based on the information, the geometry and position of routing nets can be optimized to design a routing network with minimum delay.

Key words - Very Large Scale Integration, Routing, Deep-Submicron Chip

1. Introduction:

Deep-Submicron Chips have thin wires distributed throughout the chip. The routing wires are packed very closely as the VLSI technology improves day by day. The wires of opposite polarity create unwanted transmission line effects leading to delays in analog chips and clock jitters in digital circuits. Analog circuits become unstable in the case of unmeasured signal delays. For instance a negative feedback intended to stabilize the amplifier inside a chip, will become positive feedback and make oscillations due to signal delays. The digital circuits may completely fail because of clock jitters. Synchronous digital circuits are meant to be operated upon by a common clock. Delays due to routing will virtually create an illusion as the different digital circuits are driven by different clocks. The foresaid effects can be minimized by proper frequency analysis of the transmission line networks which is the goal of this work.

2. Related Work:

[1] describes that on-chip inductive effects become pre-dominant in Ultra deep submicron (UDSM) interconnects due to increasing clock speeds and decreasing interconnect lengths. The signal waveforms are affected by noise induced by inductive effects which ultimately affects circuit performance and signal integrity. [2] explained the influence of crosstalk noise dominating in deep submicron VLSI design as interconnects are closely placed over a small

layout area. Signal response and signal integrity is severely affected by crosstalk delay and noise. An algorithm for crosstalk aware clock tree construction is designed. In [3] describes critical issues that are the outcome of shrinking feature size in deep-submicron technologies. CMOS driver is simplified as a linear circuit in which a constant resistance is used to model the nonlinear and time varying MOS resistance. The foresaid method becomes inaccurate for signal integrity analysis of high speed interconnects. Finite Difference Time Domain based method can be used for a reasonably accurate time domain analysis of non linear transmission line behavior found in deep-submicron VLSI chips.

3. Frequency Response of RLC on Radio Frequencies:

Radio Frequency Signal is an Electromagnetic Wave in the form of electrical signal in a wire. The electrical signal in the wire oscillates at the same rate as the electromagnetic wave which is inducing the electrical signal in the wire that is fed by the antenna. The electromagnetic wave propagates with a speed of $3x10^8$ m/s in free space. This space divided by the frequency of the electromagnetic wave gives the wavelength. Since the electrical signal oscillates at the same rate as the electromagnetic wave both have the same frequency. Hence the electrical wavelength of the RF signal in a wire can be calculated using Equation 1.

$$\lambda = C / f \quad (1)$$

Where

λ is the electrical wavelength of the RF signal on the conductor,

C is the speed of propagation of Electromagnetic Wave in Free Space

f is the frequency of the RF signal on the conductor

If the length of the wire carrying RF signal approaches the electrical wavelength of the signal under consideration, then the wire acts as a transmission line for that frequency component of the RF signal. Eventhough transmission line effects are present at all frequencies, the effect is more pronounced when electrical wavelength becomes more or less becomes equal to the length of the wire under consideration.

The transmission line effect in conductors is caused by parasitic resistors, capacitors and inductors along the wire carrying the signal. For analysis purpose the transmission line with lumped component effects can be modeled using distributed R,L,C elements on the per length basis. Hence these electrical parameters are provided for one meter. The performance of the transmission line calculated for one meter is converted to transmission line of any length as required. The electrical model of the signal carrying wire inside a Deep-Submicron VLSI chip is shown in Figure 1.

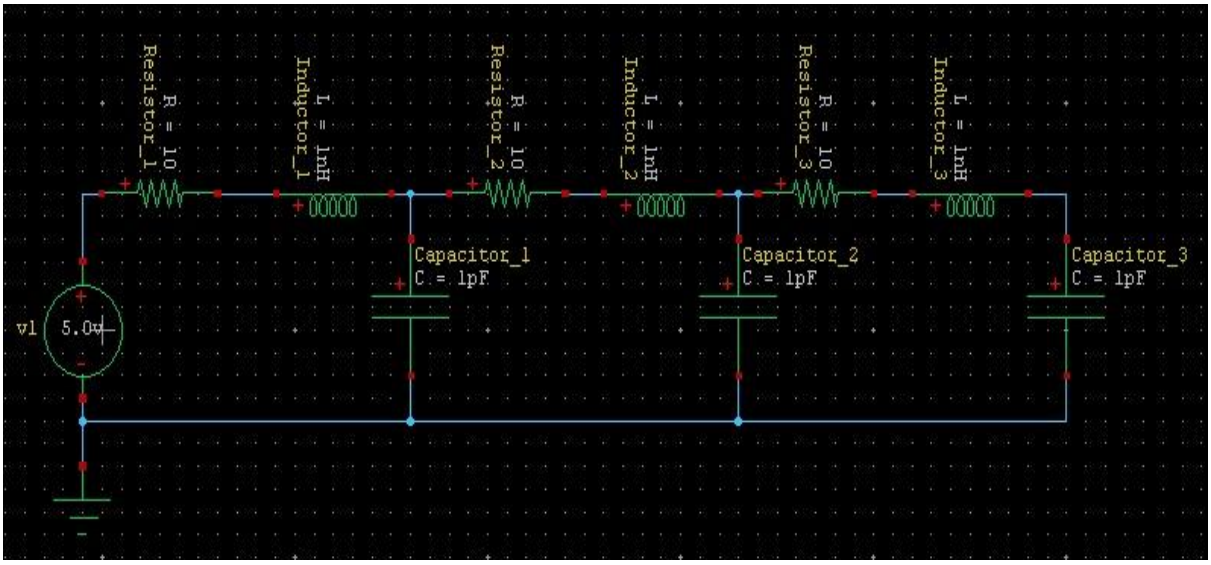

Figure 1 Wire inside Deep-Submicron VLSI Chip Modeled as a Transmission Line

4. Simulation Results:

The simulation results are shown in Figure 2. The figure clearly shows the deviation of the response from the ideal nature. It is obvious that at high frequencies the deviation is more pronounced than at low frequencies. The inference is that at high frequencies the electrical wavelength becomes very less. It is easy for even an interconnect of minimum length to exceed the electrical wave length measured and hence the result. If transmission line effect occurs, the wire starts to behave as an antenna and starts to radiate the electrical signals as electromagnetic waves. This leads to wastage of power. The frequency at which the wire operates as expected can be found from the simulation results. A compromise between the required frequency of operation and the frequency the application in hand demands is made. Not all frequency bands are open for use by consumers of electronic gadgets. Some frequency bands are licensed and are to be meant for commercial signal transmission to be used in applications like high speed wireless internet, analog and digital television broadcasting and short distance microwave links used in AM, FM radio stations. Considering all the above factors the frequency of operation required is determined. The layout and geometry of the wire can be adjusted such that it has minimum attenuation and delay at the particular frequency of operation. Exhaustive simulation tests are conducted such that the wire behaves as ideal as possible and does not radiate the electrical energy as electromagnetic waves.

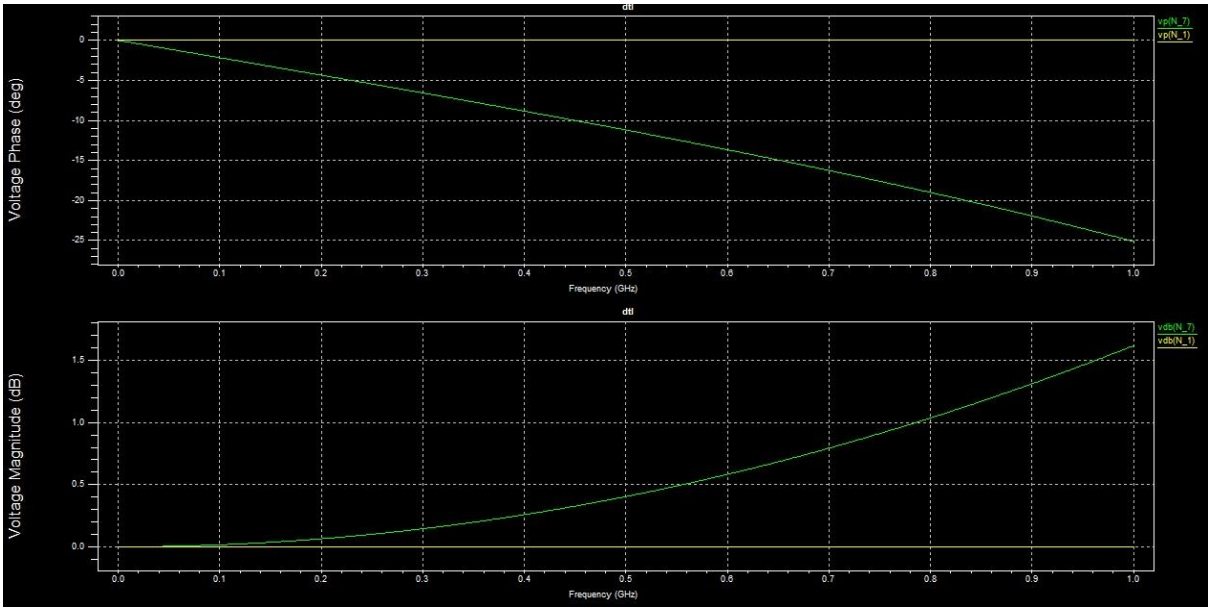

Figure 2 Amplitude and Phase response of Transmission Line model of High Speed Interconnect

5. Conclusion:

The simulation results open the possibilities of finding the range of frequencies for which the interconnect behaves as a transmission line. Signal carrying interconnects can be constructed in certain shapes of curves so that transmission line effect is reduced. The analysis can also be used for the design of analog chips operating on RF signals. In such applications the transmission line effect has to be purposefully introduced for impedance matching between the feeder line and the antennae input. Once the impedance matching is done, the antenna together with the matching network acts as a resonator thereby operating with full efficiency.

References:

[1] Ravindra, J. V. R., Pandurangaiah Yagateela, and Narasimha Prasad. "A Novel Analytical Model for Analysis of Delay and Crosstalk in Non Linear RLC Interconnects for Ultra Low Power Applications." Computer Modelling and Simulation (UKSim), 2013 UKSim 15th International Conference on. IEEE, 2013.

[2] Samanta, Tuhina, et al. "Crosstalk aware coupled line delay tree construction for on-chip interconnects." Quality Electronic Design (ISQED), 2011 12th International Symposium on. IEEE, 2011.

[3] Li, Xiao-Chun, Jun-Fa Mao, and Madhavan Swaminathan. "Transient analysis of CMOS-Gate-Driven interconnects based on FDTD." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 30, No. 4, pp: 574-583, 2011.

[4] Kar, R., et al. "An accurate crosstalk noise estimation method for two simultaneously switched on-chip VLSI distributed RLCG global interconnects." Signal and Image Processing (ICSIP), 2010 International Conference on. IEEE, 2010.