Non-Linear Test Pattern Generation For Stuck At Fault Identification

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Abstract

For identifying the fault the test pattern generation is the major role in VLSI design. The pseudo random generator that is linear/Non linear shift register are utilized to produce the patterns and given the circuits. In this paper Non Linear Feedback shift registers are used over Automatic Test Pattern Generation to identify the Stuck at faults which offers less power compare to the conventional method with high fault coverage. The proposed method is simulated and verified using Xilinx ISE tool.

Keywords: VLSI, Non linear feedback shift register, stuck at fault, Xilinx ISE.

1. Introduction

While chip designing the testing is the major role due to increase in the circuit complexity which reduce the fault in the circuits. In [1] a system architecture for failure identification problem in mobile robots is described. Multiple Model Adaptive Estimation is utilized. In [2] single fault theorem are utilized for combinational and sequential circuits to identify the faults is described. In [3] an algorithm is used to check the every fault pair to verify the equivalence/distinguishing vector is described. In [4] Redundancy removal and redundancy Identification are algorithms are used to enlarge the equivalence based logic optimization applications. In [5] limited broad side transition ATPG technique is described to overcome the faults.

3. Proposed Method

In ATGP process the fault target is consist of two parts namely fault activation and fault propagation. A signal which is reverse to the fault model value. By path sensation technique fault propagation onwards the output signal. Figure 1 shows the design of Non Linear Feedback Shift Register.

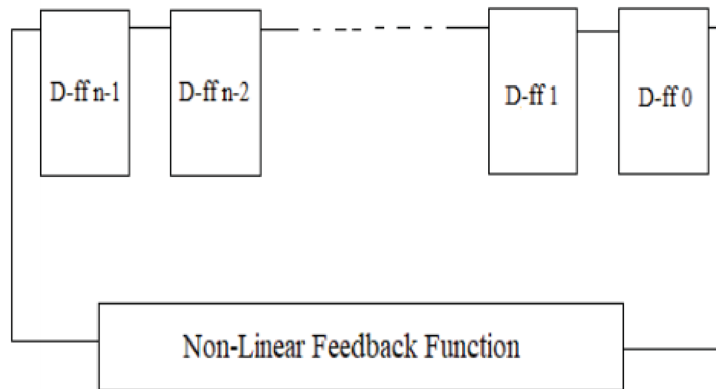

Figure.1 Design of Non linear feedback shift register.

The above design is made up of series of D FlipFlop and in the feedback logic AND gate attached with the XOR gate. To generate the sequence of output the primary input is the major part. After one full cycle ends the this sequence with repeat which is referred as sequence period. Without generating the sequence state shift register seed should never be zero. At the gate input, the faults are injected in to the circuits. In the input the OR gate are located to inject the stuck at 1 fault similarly AND gate is located to inject the stuck at 0 fault. In this paper the Non linear method s realized. For every circuit the nonlinear method is structures on the basis of the number of inputs. Higher pattern number is produced on the basis of the primary selection seed is done.

5. Results and Discussion

The proposed design is implemented in Xilinx ISE tool. The simulation is implemented for benchmark circuits ISCAS'89. Figure 2 shows the simulation result for the circuit without fault and figure 3 shows the simulation result with fault injected circuit.

Figure.1 simulation result without fault in the circuit

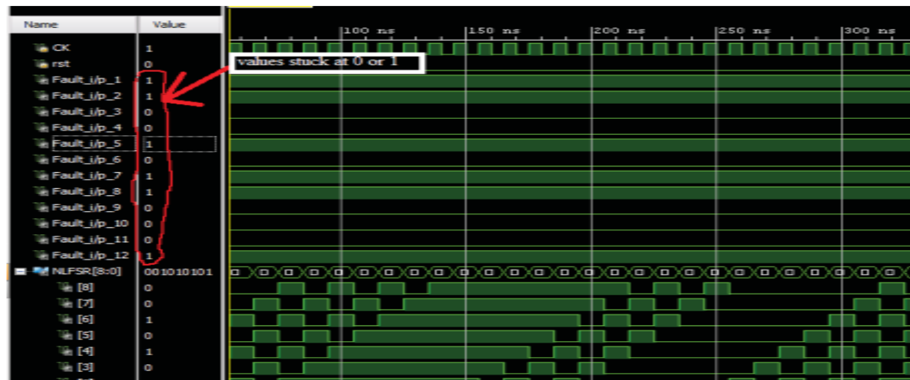

Figure.2 Simulation result with fault injected in the circuit

The above figure shows that the fault injected input does not vary on the values I remains stuck at 1 or 0.Figure 3 shows the performance analysis of the before and after fault injection in the circuit. Before injecting the fault the circuit occupies 5.47 µw power and after the injection of fault the power is 18.69µw.

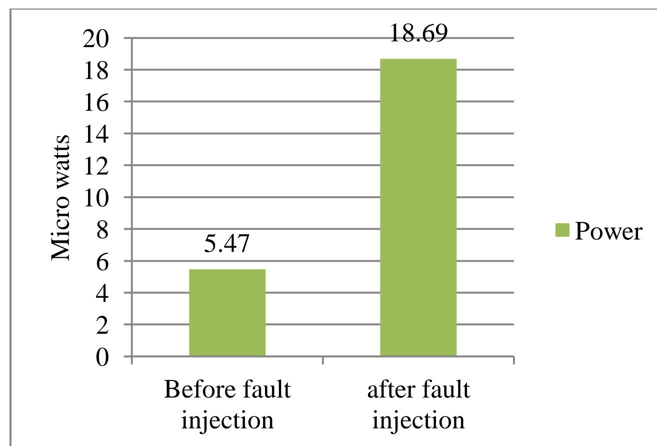

Figure. 4 Performance analysis of power for before and after fault injection

Figure 4 shows the performance analysis of the Linear Feedback shift register and Non linear feedback shift register. In this the total power occupied for the linear method is 5.47 µw and for the non linear provides 0.098µw.

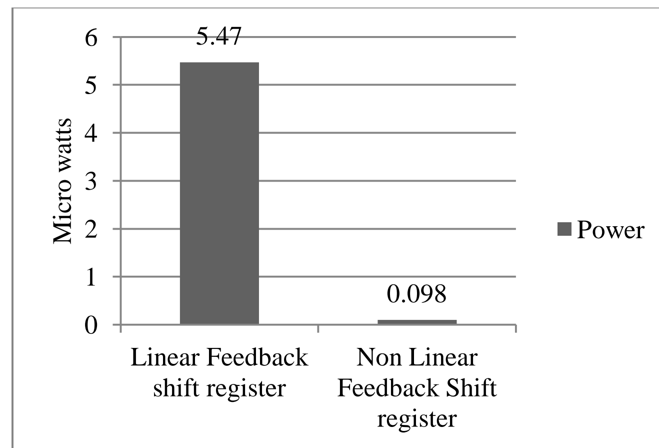

Figure.4 Performance analysis of the 4-bit Linear shift feedback register and Non linear Feedback shift register.

6. Conclusion

In this paper the Non Linear feedback shift register test pattern generation are used to identify the stuck at fault. This method is implemented using Xilinx ISE tool. Compare to the 4-bit linear method the nonlinear method offers 98.07% less power.

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