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Design and Implementation of Power Efficient Modified Russian Peasant Multiplier using Ripple Carry Adder

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Abstract: FIR filters, microprocessor and digital signal processor are the core system of multipliers. MAC is the most important building block in DSP system. The key element of high throughput multiplier and accumulator unit (MAC) is to achieve a high-performance digital signal processing application. In this paper, Modified Russian Peasant Multiplier (MRPM) using Ripple Carry Adder (RCA) has been proposed. According to Russian Rule's, Divide and conquer technique is used in the multiplication process. But, in perspective of digital design, only shifters and adders are used in Russian Peasant Multiplier to produce Partial Product Generation (PPG). A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. Here, ripple carry adder is used for low power application. Reducing the chip size, increasing the speed and reducing the power consumption are main crucial factors in VLSI System design environment. The goal of this research work is to design the VLSI implementation of MAC for high-speed DSP applications. For designing the Multiplication and accumulation unit, different kinds of multipliers and adders are considered in this paper. The total operation is coded with Verilog HDL using ModelSim 6.3C, synthesized by using Xilinx ISE 12.4i design tool.

Keywords: Modified Russian Peasant Multiplier (MRPM), Ripple Carry Adder (RCA), Partial Product Generation (PPG), Verilog Hardware Description Language (Verilog HDL), and Multiplication and Accumulation unit (MAC).

1. Introduction

Multiplication is mostly utilized in applications for signal processing, graphics and scientific computation. The different advanced designs of multipliers have been designed for higher speed, low latency and lower power consumption at lesser chip area. Thus the high speeds, low power VLSI implementations can be achieved. These three parameters such as power, area and speed are always main traded off to achieve. The two basic operations involved in multiplication process are the creation of partial products and their accumulation. Addition is one of the foremost normally used mathematical processes in digital signal processor, it also can be used as a building block for synthesis of all alternative arithmetic operations. Therefore, the

economical implementation of associate degree arithmetic unit is bothered; the binary adder structure becomes an essential hardware unit.

The design of a low power high speed Russian peasant multiplier and its implementation on reconfigurable hardware has been proposed. For arithmetic multiplication, the different types of multiplication architectures like array multiplier, Booth multiplier, Wallace tree multiplier and Booth Wallace multiplier and Russian peasant multiplier have been analyzed. Then it has been found that Russian peasant multiplier is most efficient , providing optimum delay, power and area for multiplication. Low power modified Russian peasant multiplier using ripple carry adder have been used to reduce power and delay.

In modern digital signal processing, Multiply-accumulate operation is one of the basic arithmetic operations. The MAC unit provides high-speed multiplication, multiplication with cumulative addition, multiplication with cumulative subtraction, saturation functions. Hence, the main aim is to examine different pipelined MAC architectures and circuit and the design techniques which are suitable for the implementation of high speed signal processing algorithms. Hence, a high-speed MAC that is capable of supporting multiple and parallel operations is highly sensible. MAC is composed of an adder, multiplier and an accumulator. The implementation of the multiplier is in the form of Russian peasant Multiplier. The adder used is Ripple Carry Adder. Figure 1 shows the basic structure of MAC unit.

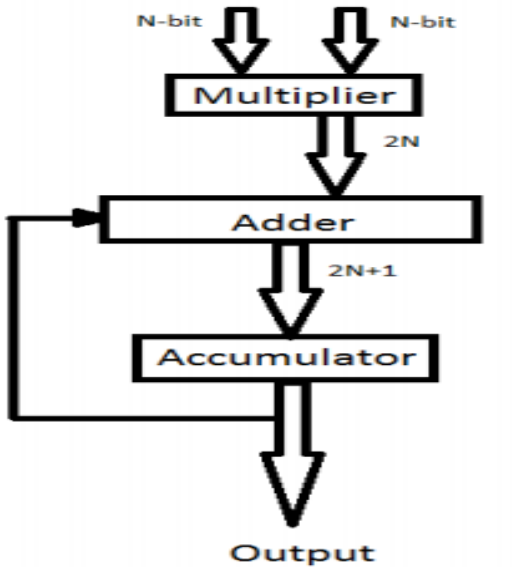

Figure 1. Basic MAC unit

All DSP algorithms would need some form of the Multiplication and Accumulation Operation. It is consists of an adder, multiplier and the accumulator. Usually adders implemented in DSPs are Ripple Carry Adders, Carry-Save or Carry-Select adders. Basically the multiplier will multiply the input values and give the results to the adder, which will add the multiplier results to the previously accumulated results. In this paper, modified Russian peasant multiplier using ripple carry adder has been designed. The reason for using the Russian peasant multiplier is that, using this multiplier can reduce the number of partial products during multiplication. The adder here have used is ripple carry adder. This adder has a very simple architecture and is very easy to implement. This architecture which is used to reduce the area, delay, power and the improve the speed.

2. Literature Survey

In [Chang.T.Y. and Hsiao, M.J., 1998] described the carry select adder using single ripple carry adder. a carry-select adder that requires a single carry-ripple adder with zero carry-in, an add- one circuit, and a multiplexer. Having a lower transistor count and 1.5 more units of two-input NAND gate delay, the add-one circuit is used to replace the original carry-ripple adder with carry- in Cin = 1. The transistor count can be reduced by 29.2% with a speed penalty of 5.9% for n = 64.In [Gunasekaran, K., and Manikandan, M, 2014], Reconfigurable FIR filter has been designed by using Russian Peasant Multiplier (RPM). For performing addition operation of MAC unit, Carry Select Adder (CSLA) with Sklansky Adder is used in the design. It offers 30.9% reduction of area than traditional CSLA. Further to improve the architecture, some changes are made in CG block of CSLA architecture.

In [Elguibaly, F, 2000] explained a fast parallel multiplier –accumulator using modified booth algorithm. A dependence graph (DG) to visualize and describe a merged multiply-accumulate (MAC) hardware depend on the modified Booth algorithm .The carry-save technique is used in the Booth encoder, and the accumulator sections to ensure the fastest implementation. The DG applies to any MAC data and allows designing multiplier structures that are normal and have minimal delay, sign-bit extensions, and data path width. Using the DG, a fast pipelined implementation is proposed, in which an accurate delay model for deep submicron CMOS technology is used. The delay model explains multi-level gate delays, taking into account input ramp and output loading.

In [Saikumar, M., et al. 2014] described the design and performance analysis of multiply –accumulate (MAC) unit. Multiply-Accumulate (MAC) unit is designing for various high performance applications. MAC unit is a fundamental building block in the computing devices, especially Digital Signal Processor (DSP). MAC unit operates multiplication and accumulation process. MAC unit consists of multiplier, adder, and accumulator. In the traditional MAC unit model, multiplier is designed using modified booth multiplier. In this paper, MAC unit model is designed by incorporating the various multipliers such as Array Multiplier, Ripple Carry Array Multiplier with Row Bypassing Technique, Wallace Tree Multiplier and DADDA Multiplier in the multiplier module and the performance of MAC unit models is analyzed in terms of area, delay and power.

In [Fang, C.J., et al, 2002] presented the fast and compact dynamic ripple carry adder design. Adders are building blocks and constitute part of the critical path. In this paper, proposed high-speed ripple carry adder designs using dynamic circuit techniques. The simulation result shows that the proposed dynamic ripple carry adders are at least two times faster than the existing static ripple carry adder. Further all of the proposed designs compare to the previous dynamic ripple carry adder design that employs the DCVS logic.

3. Ripple Carry Adder

A ripple carry adder is simply full adder connected in a series so that the carry must propagate through every full adder before the addition is completed. Multiple full adder circuits can be cascaded in parallel to sum of an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. The logic circuit of ripple carry adder in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into another stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not used until the carry in of that stage occurs. Propagation delay is time elapsed between the application of an input and occurance of the corresponding output. Consider a NOT gate, When the input is "0" the output will be "1" and vice versa. The time taken for the NOT gate's output to become "0" after the application of logic "1" to the NOT gate's input is the propagation delay. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurance of the carry out (Cout) signal. Circuit diagram of a 4-bit ripple carry adder is shown below. Figure 2 shows the 4-bit ripple carry adder.

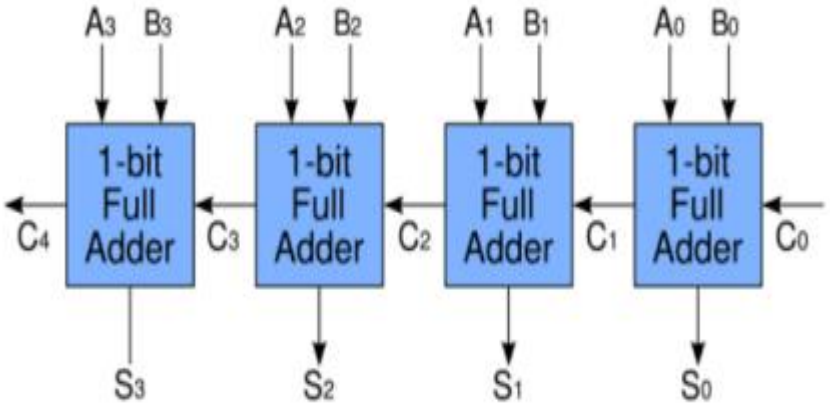

Figure 2. 4-bit Ripple Carry Adder

4. Russian Peasant Multiplier

Russian Peasant Multiplication (RPM) is a easy way to multiply the two 'n' bit multiplication. Russian peasant multiplier based on dividing and multiplying by two. Russian Peasant Multiplier consists of Shifters, 2:1 Multiplexer and adder unit. It is a easy and simple

architecture which consumes less area and delay for computation of multiplications. When compared to the other multiplier, Russian Peasant Multiplier provides less Area, Power and Time product. RPM based multiplier gives the partial product results without help of FAs and HAs; instead it uses the multiplexers for generating the PPG results. Architecture of 8-bit Russian Peasant Multiplier is shown in Figure.3. In Figure 3, the Shifters and Multiplexers are used to find the partial product results which consume less area and power than other multiplier. Further Wallace Tree Reduction is used in RPM based multiplier for reducing the complexity of PPG.

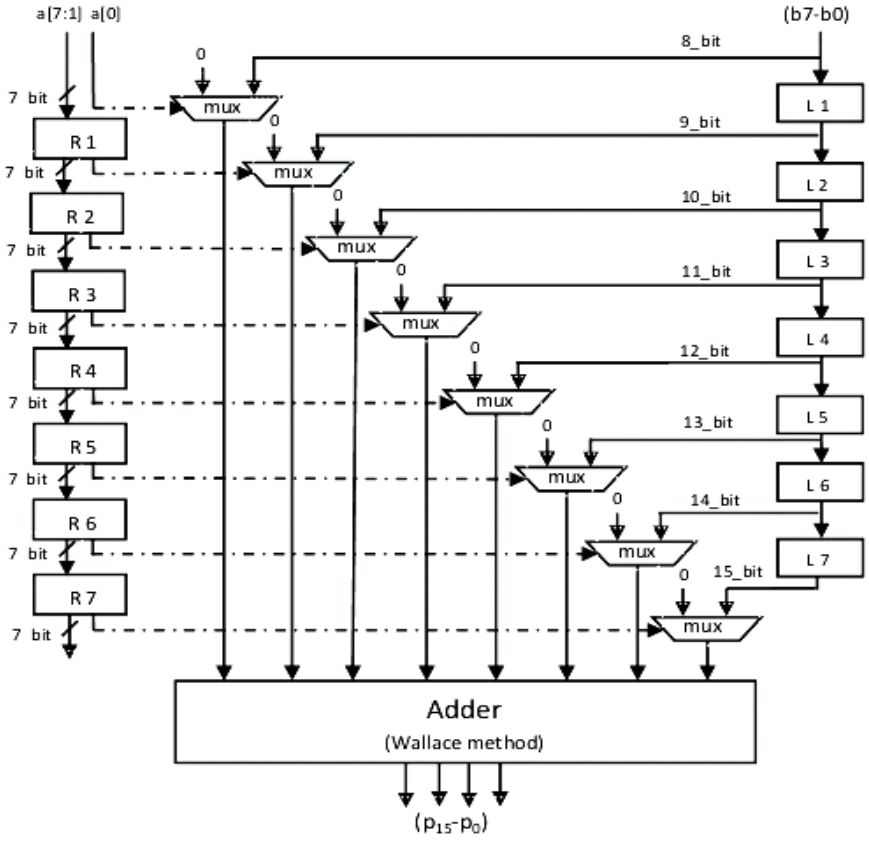

Figure 3.Architecture of 8-bit Russian Peasant Multiplier

5. Modified Russian Peasant Multiplier

In this paper, Modified Russian Peasant Multiplier is designed to improve the hardware utilization of the circuit. The main aim of VLSI System design is to reduce the hardware complexity, power consumption and to increase the speed & throughput of the system. Hence, the aim of proposed work is reduce the delay and power consumption of multiplication.
In general, Multiplication function has three important steps:

- **Partial Product Generation (PPG)**

- **Wallace Tree Reduction (WTR)**
- **Partial Product Addition (PPA)**

In the place of PPG generation, MRPM circuit is developed in the proposed work. The architecture of modified Russian peasant multiplier has been illustrated in Figure.4. It gives 'n' rows of partial products using only 'Multiplexers'.

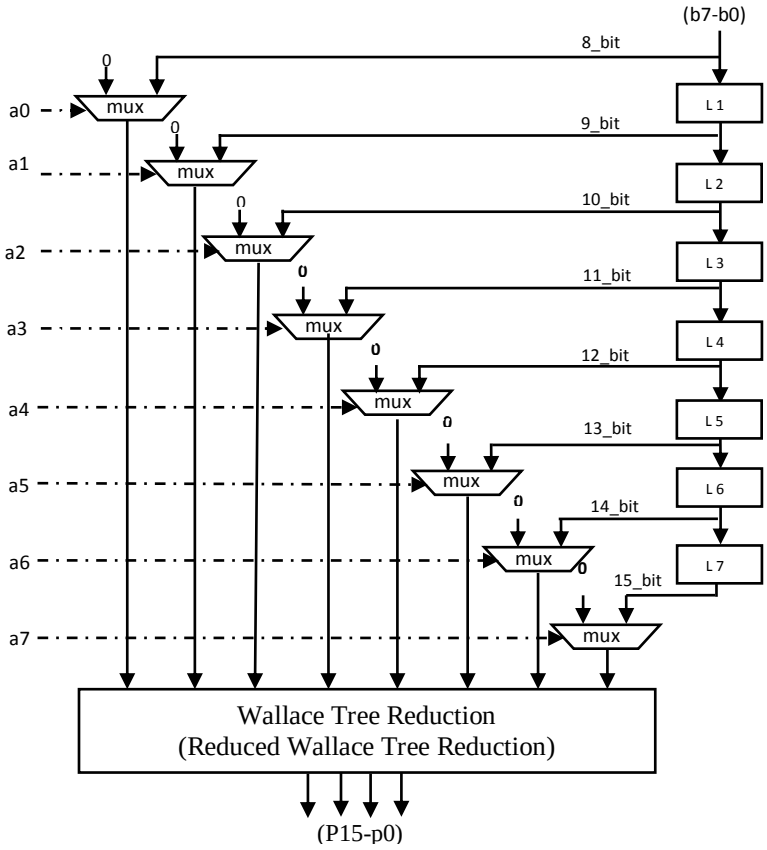

Figure 4. Architecture of Modified Russian Peasant Multiplier

6. Proposed Modified Russian Peasant Multiplier using Ripple Carry Adder

In this paper, Modified Russian Peasant Multiplier using Ripple Carry Adder has been proposed. In Russian Peasant Multiplier, Wallace tree method has been reduced which is called as "Modified Russian Peasant Multiplier". The modified Russian peasant multiplier using ripple carry adder, which is used to improve the hardware performance of the circuit. To reduce the 'n' rows of partial product values into two rows, WTR methods have been used in general.

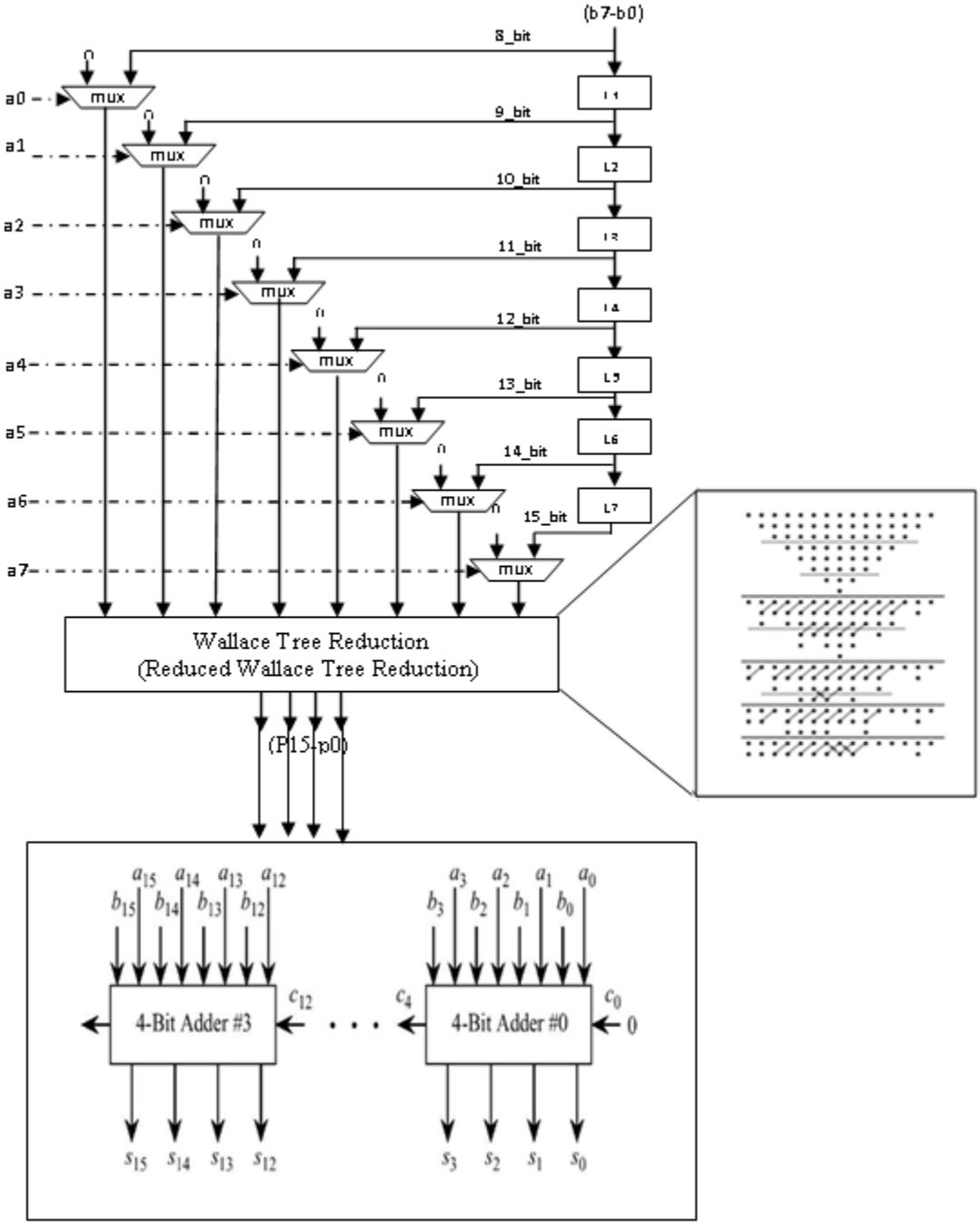

Figure 5. Architecture of proposed MRPM using 16-bit Ripple carry adder.

But in the proposed MRPM structure, Reduced Complexity Wallace Reduction (RCWR) has been used (as shown in Figure.5). As shown in Figure.5, the final stage of RWTR requires an

efficient adder (2*n-bit adder) to perform the addition process. In the place of addition part "Ripple Carry Adder (RCA)" has been used in the proposed work. Hence, the proposed MAC unit named as Ripple Carry Adder based MRPM.

7. Results and Discussion

Simulation result of proposed MRPM using Ripple Carry Adder has been validated by using ModelSim 6.3C tool. The synthesis result has been validated by using Xilinx ISE 12.4i design tool. The simulation result of existing Russian peasant multiplier is shown in Figure 6. The simulation result of ripple carry adder is shown in Figure 7. The simulation result of MRPM using Ripple Carry Adder is shown in Figure 8 .

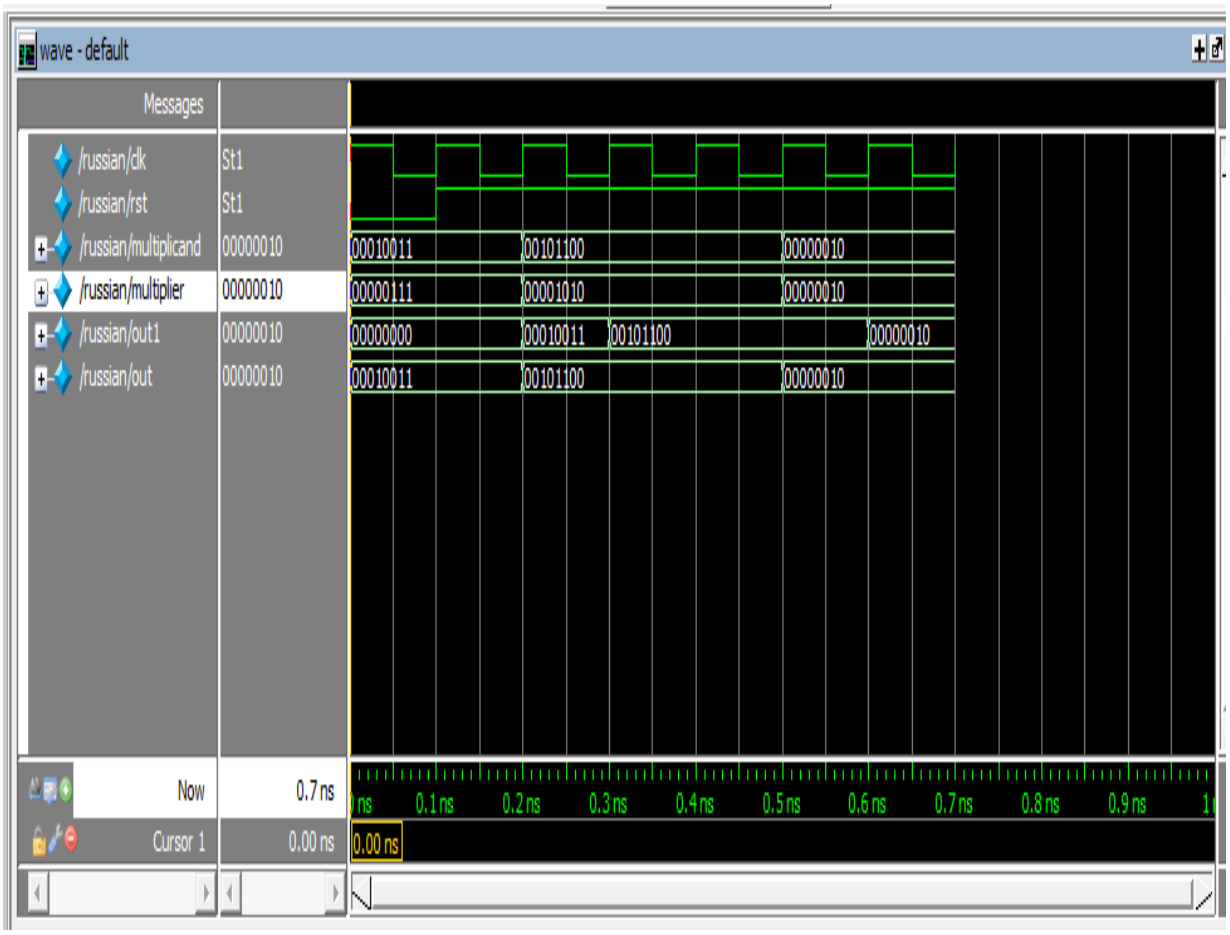

Figure 6.Simulation result of existing Russian peasant multiplier

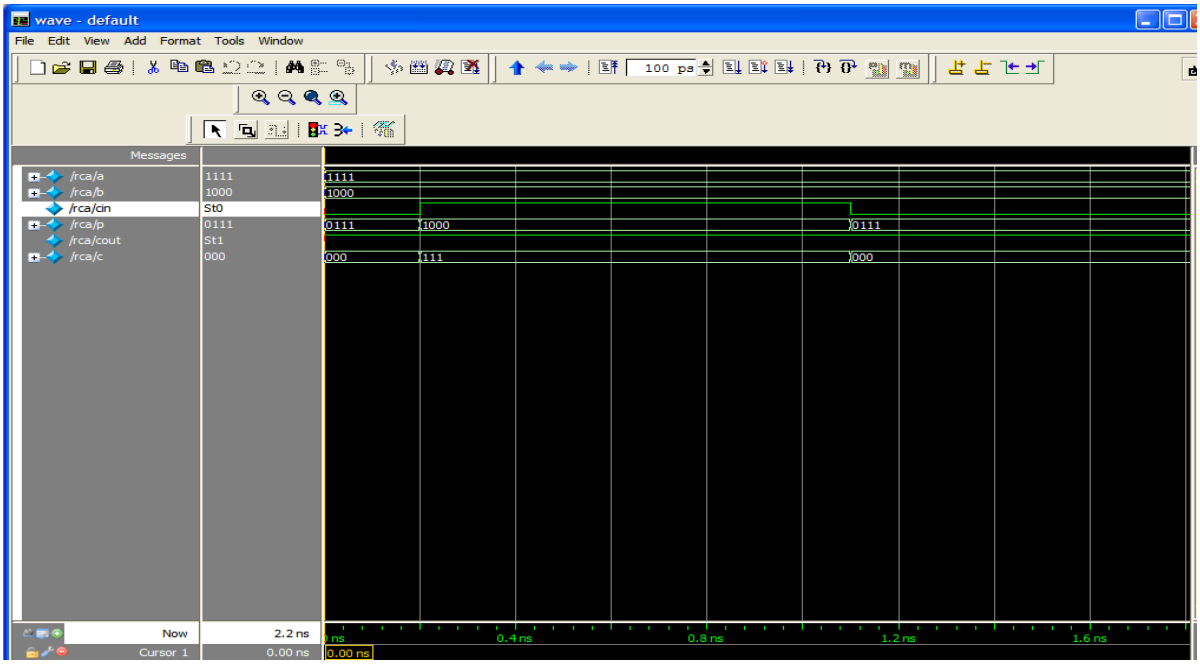

Figure 7.Simulation result of Ripple carry Adder

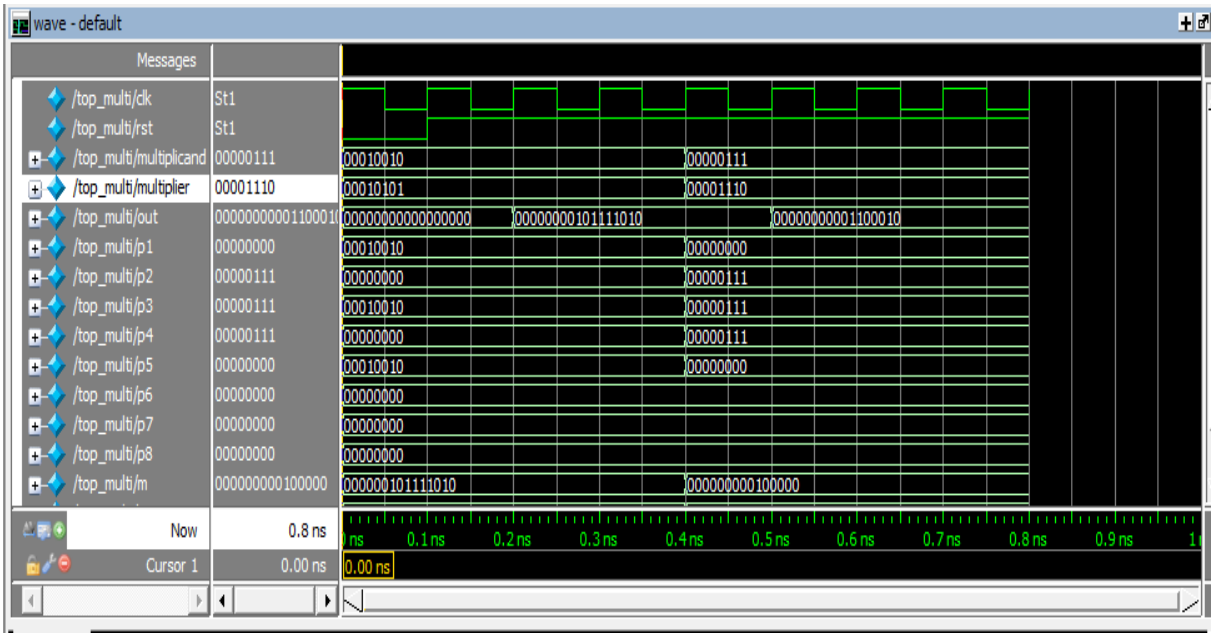

Figure 8.Simulation result of MRPM using ripple carry adder

Table 1. Comparison of existing Russian peasant multiplier and proposed MRPM using Ripple Carry Adder

Types/Parameters	Slices	LUTs	Delay (ns)	Power (W)
Existing Russian Peasant Multiplier	93	182	31.469	1.515
Proposed MRPM using Ripple Carry Adder	88	161	18.646	0.031
Percentage reduction%	5.37	14.2	40.7	97.9

Table 1 shows the Comparison of existing Russian peasant multiplier and proposed MRPM using Ripple Carry Adder. When compared to existing method, the proposed modified Russian peasant multiplier provides better performance. The performance evaluation of existing Russian peasant and proposed MRPM using ripple carry adder is shown in Figure 9.

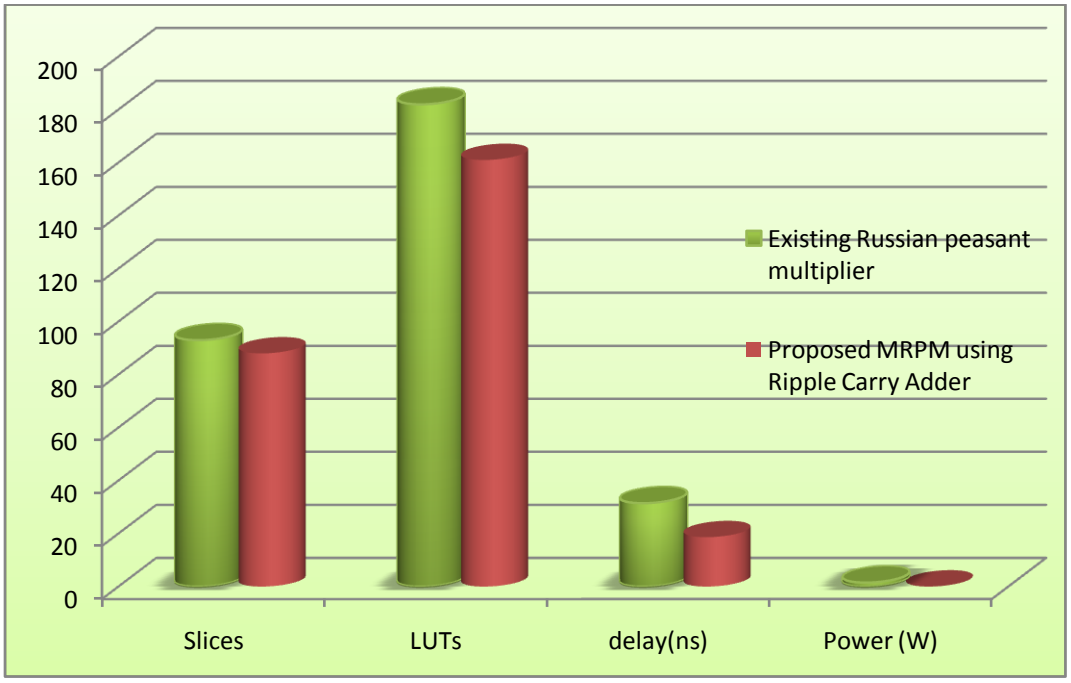

Figure 10.Performance evaluation of existing Russian peasant and proposed MRPM using ripple carry adder

8. Conclusion

In this paper, Modified Russian Peasant Multiplier using Ripple carry adder has been designed by using Verilog Hardware Description Language (Verilog HDL). For the Partial Product Generation (PPG), Proposed MRPM unit is used with the help of only "Multiplexers". For the Wallace Tree Reduction (WTR), Reduced Complexity Wallace Tree Reduction (RWTR) unit is used with the help of only "Full Adders". Hence, the proposed Multiplication and Accumulation unit (MAC) is named as "Modified Russian Peasant Multiplier using Ripple carry adder" unit. The proposed MAC unit offers 5.37 % reduction in Slices and 14.2 % reduction in LUTs and 40.7 % reduction in delay and 97.9% reduction in power consumption than existing Russian peasant multiplier. In future, Proposed MAC unit offers great advantage in minimizing the chip size for designing the communication standards.

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