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Cascaded H-Bridge Seven Level Inverter using Carrier Phase Shifted PWM with Reduced DC sources

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Abstract

This paper presents a multi level inverter with seven level voltage generation scheme using cascaded H-bridge MLI topology utilizing reduced number of DC sources. By utilizing switched capacitor methodology the number of DC sources required to generate seven levels is minimized. Three numbers of H-bridges are employed in seven level generations where only one dc source is used and in the remaining bridges only capacitors are used along with a unidirectional switch for capacitor charging. This paper utilizes a multi carrier PWM technique based on phase shifted carrier for generating pulses to get seven level output. This paper also discusses the switching schemes for charging switches used and there is a small dip in efficiency of this inverter due to the existence of power loss which occurs during charging and discharging the capacitors. The advantage of this inverter is it can produce an output voltage higher than the input voltage in the ratio 1:3 and also the output voltage have lesser harmonics than conventional square and quasi square wave inverters due to multilevel output voltage. The proposed multi level inverter using single DC source and three cascaded h bridges using carrier phase shifted sine PWM technique is implemented in MATLAB/Simulink platform and merits of the proposed inverter system is verified through simulations.

Keywords: Cascaded H-Bridge multi level inverter (CHB-MLI), Multi Carrier Phase Shifted Sinusoidal Pulse Width Modulation (CPS-SPWM)

1. INTRODUCTION

In recent years most of the researches are carried on multi level inverter topologies which can generate an output voltage closer to sine wave without the use of LC filters. MLI produces a high power output with voltage and current profile containing lesser total harmonic distortion compared to classical two level inverters. MLI's are classified into diode clamped,

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flying capacitor and cascaded H bridge based on the structure and components used in the circuit. Diode clamped and flying capacitor topologies have complex control technique and use uncontrolled diodes for voltage clamping to provide different voltage levels and balancing voltage across capacitors is a difficult task. But cascaded MLI's are simple in structure and also easy to control. The only disadvantage of the cascaded MLI converter is it requires n number of isolated dc sources to produce 2n+1 level output voltage. Therefore topology advancements are required in this type of multilevel inversion system with reduced dc sources and also to reduce the count of power switches and diodes used.

Multi level inverter topology with reduction of dc sources based on switched capacitor techniques with normal dc source and single z-source network is presented in [1-2]. Multi level inverter topologies with increased voltage level based on series and parallel combination of switched capacitor network is given in [3-6]. MLI's proposed for a photovoltaic power generation [4] scheme for interfacing with ac micro grids [6]. Cascaded Multi level inverters with reduced number of power switches is presented in [7-9] for induction motor applications with wye connection and also for open winding connection. Multi level inverters for PV powered grid interfaced applications are presented in [10-12] with and without galvanic isolation between PV power and ac loads. This paper presents a new multi level inverter with seven level voltage generation scheme using cascaded H-bridge MLI topology utilizing reduced DC sources count. By utilizing switched capacitor methodology the number of DC sources required to generate seven levels is minimized. Three numbers of H-bridges are employed in seven level generations where only one dc source is used and in the remaining bridges only capacitors are used along with a unidirectional switch for capacitor charging. The operation of the proposed MLI circuit and pulse generation using CPS-SPWM is explained in the following sections.

2. Overall Configuration of Proposed System

Overall configuration of the proposed multi level conversion system is shown in fig 1. The proposed system consists of a multi level voltage generation scheme which has twelve power switches with reverse voltage blocking capability, single DC source and two capacitors with charging switches. Efficiency of the proposed scheme is slightly lesser than the conventional topology which has three dc sources due to the charging loss of capacitor. The proposed MLI converter employs a carrier phase shifted PWM where the ratio between carrier frequency and sine wave frequency is smaller which further improves the harmonic profile of the MLI converter system. A MATLAB Simulink model is developed to verify the merits of proposed new Seven Level circuit topology with single dc source using carrier phase shifted PWM and the results are presented in this paper.

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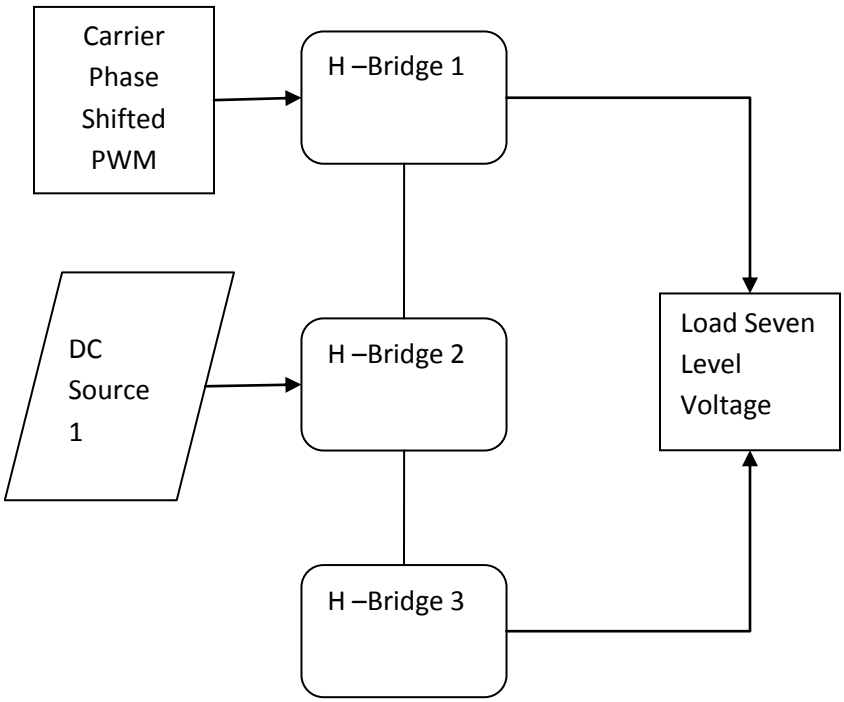

Fig 1.Overall Configuration of Cascaded MLI

3. Cascaded seven level inverter with Single DC source

By Applying a switched capacitor methodology a single input dc source seven level inverter topology is presented using cascaded MLI. The proposed circuit topology uses three H-bridges as shown in the fig 2. In which a single bridge is directly powered from a constant dc source and the other two bridges are powered through switched capacitors from the same source.

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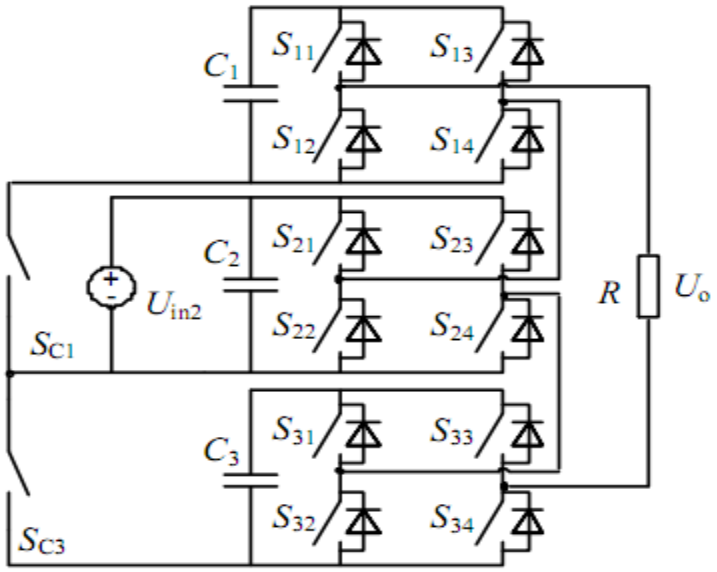

Fig 2.Circuit Diagram of Cascaded Seven Level inverter with Single DC source

4. Carrier Phase Shifted PWM

In this PWM technique sine wave is compared with multi carrier waves to generate switching pulse for producing multi level output voltage using single dc source cascaded H bridge inverter and the key waveforms are shown in fig 3. In order to generate pulse for charging switch S_{c1} pulse generated for switches S_{21} and S_{13} are multiplied using and logic. Similarly for charging switch S_{c2} pulse generated for switches S_{23} and S_{31} are multiplied using and logic.

5. Simulation Results and Discussions

Cascaded MLI using single dc source to generate seven level load voltages is simulated in MATLAB/Simulink platform and the results are presented in this section. Simulation parameters are given in Table I. Overall circuit implementation in MATLAB software is shown in the fig 4. The seven level load output voltage using proposed inverter scheme is shown in fig 5. And harmonic content in load voltage is shown in the percentage of total harmonic distortion in fig 7. Voltage across capacitors $(C_1$ and $C_2)$ is shown in fig 6.

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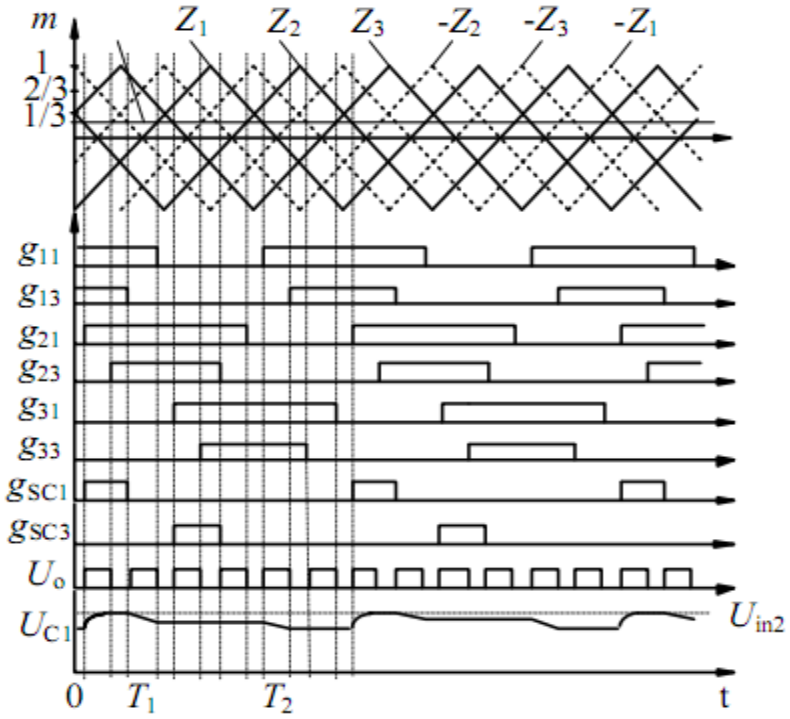

Fig 3.PWM generation using CPS-PWM

TABLE 1 SIMULATION PARAMETERS

Load PARAMETERS	
Name	Range
Resistance	10 ohms
Inductance	2 mH
Circuit parameters	
Capacitors(C_1, C_2, C_3)	2200 uF
Input voltage Uin_2	100 v DC
Output Voltage U_o	300 v AC

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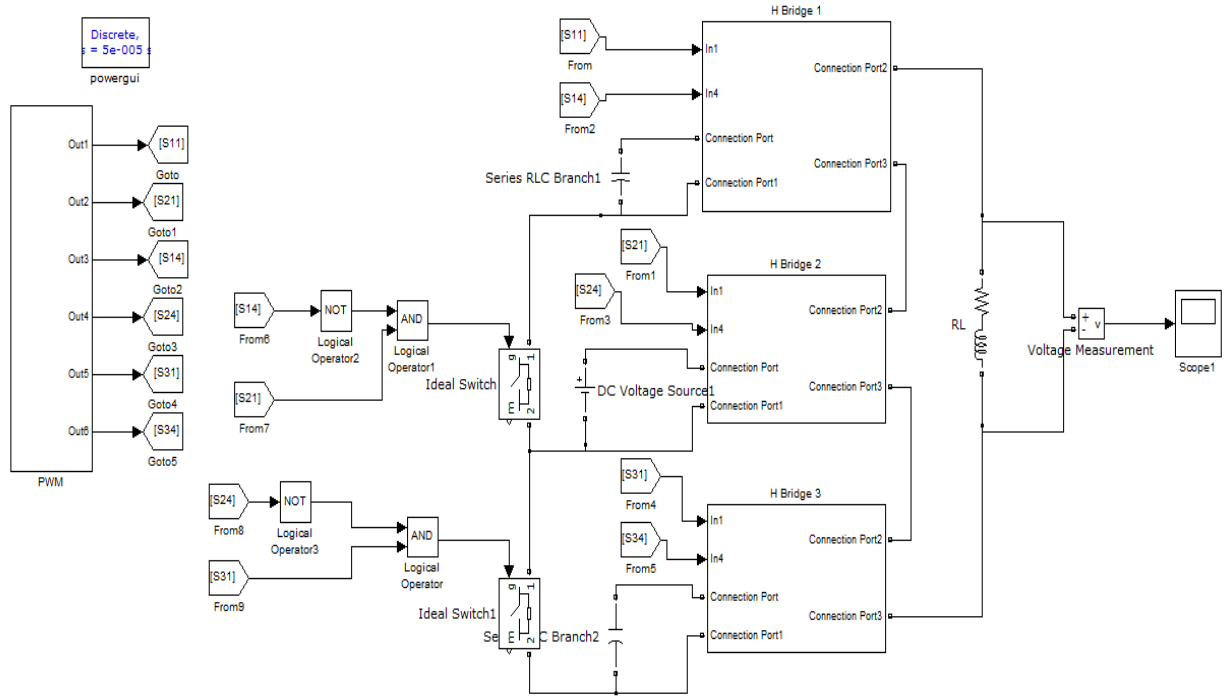

Fig 4.Matlab Implementation of Single DC source Cascaded Seven level inverter

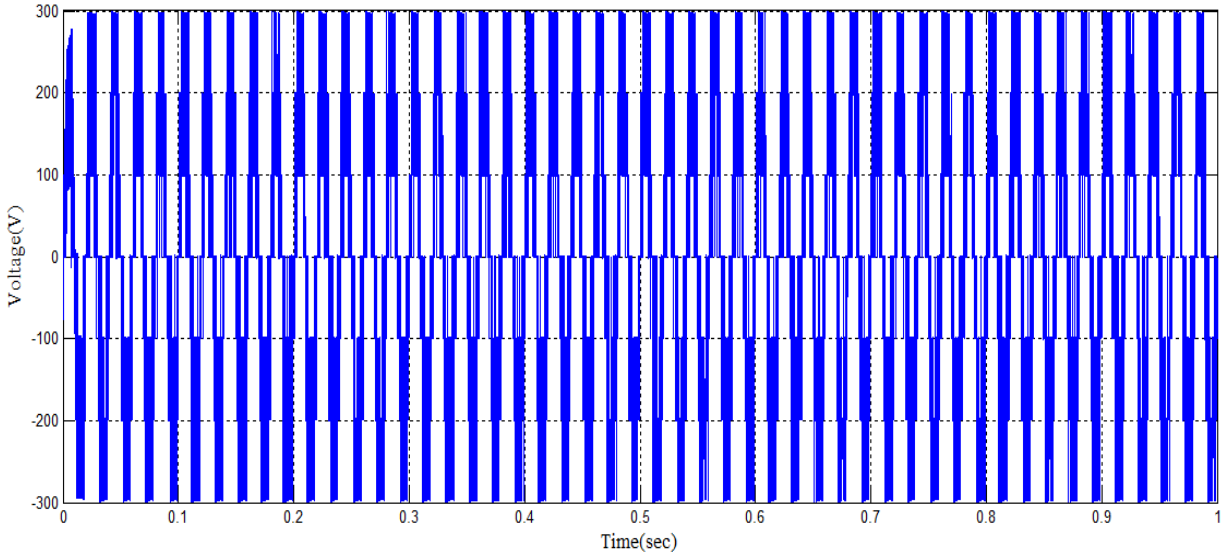

Fig 5.Seven Level load Voltage waveform

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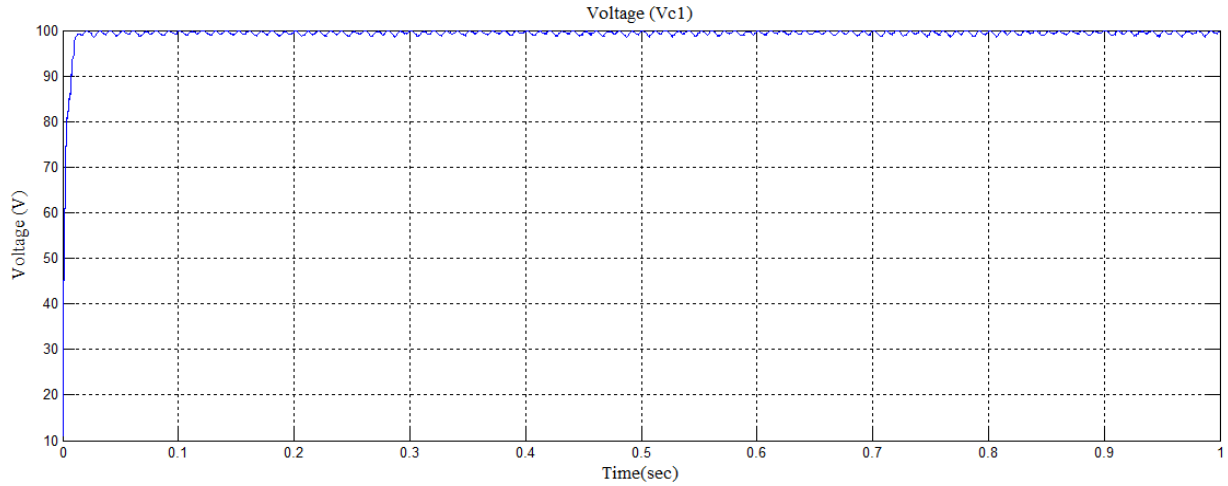
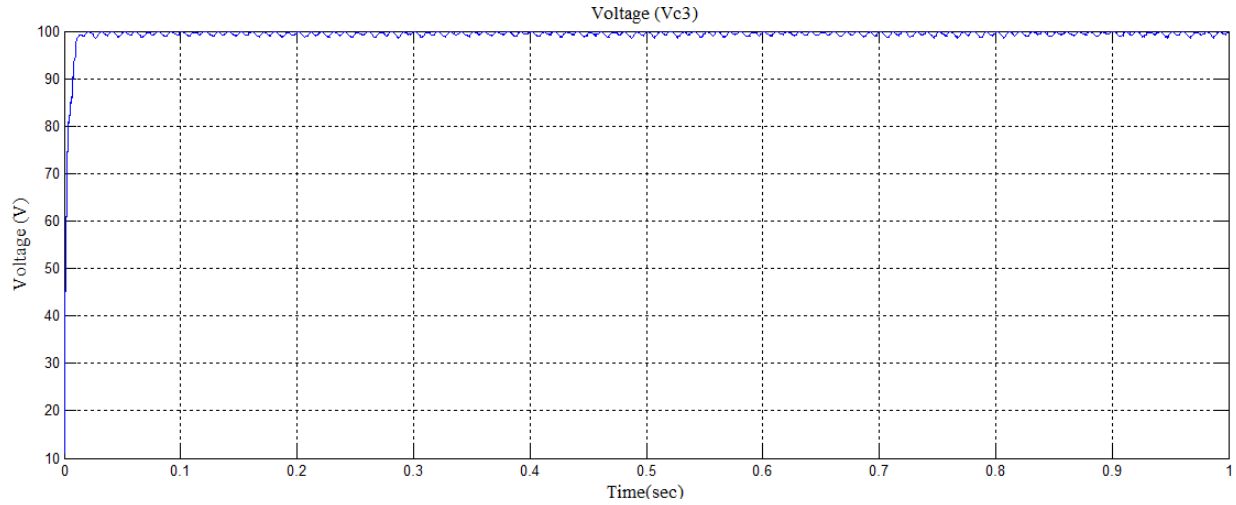


(A)



(B)

Fig 6.Dc link voltage waveform (A) voltage across capacitor vc1 (B) voltage across capacitor vc2

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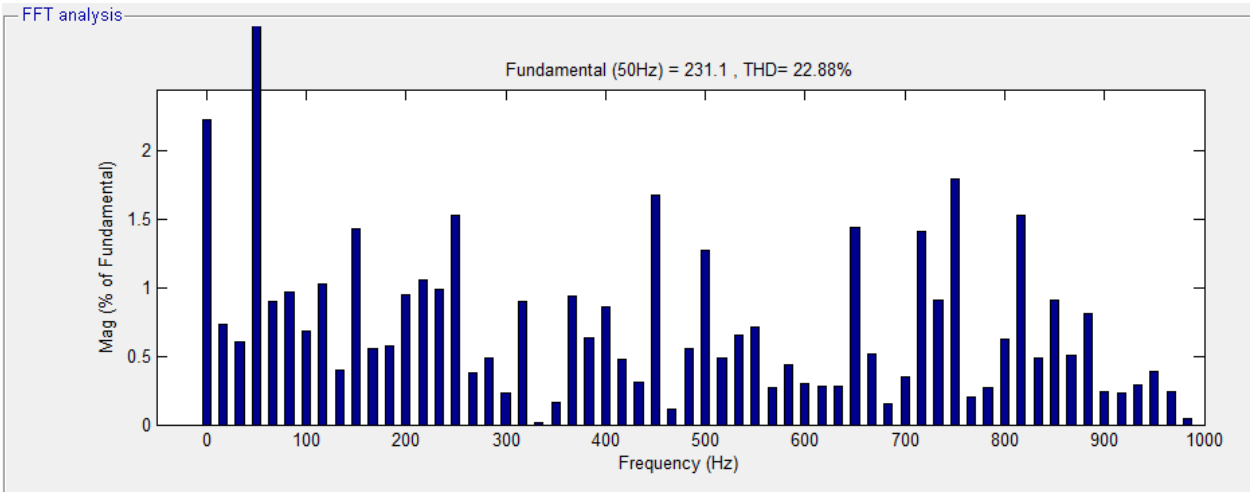

Fig 7.THD performance of Single DC source cascaded Seven Level inverter

S. No	PWM technique	THD (%)
1	LS-PWM	23.08
2	CPS-SPWM	22.06

6. Conclusion

This paper presented a new multi level inverter with seven level voltage generation scheme using cascaded H-bridge MLI topology utilizing reduced DC sources, by utilizing switched capacitor methodology the number of DC sources required to generate seven levels is minimized. Three numbers of H-bridges are employed in seven level generations where only one dc source is used and in the remaining bridges only capacitors are used along with a unidirectional switch for capacitor charging. This paper utilizes a multi carrier PWM technique based on phase shifted carrier for generating pulses to get seven level output. This paper also discusses the switching schemes for charging switches used and there is a small dip in efficiency of this inverter due to the existence of power loss which occurs during charging and discharging the capacitors. The advantage of this inverter is it can produce an output voltage higher than the input voltage in the ratio 1:3 and also the output voltage have lesser harmonics than conventional square and quasi square wave inverters due to multilevel output voltage. The proposed multi level inverter is based on single DC source and three cascaded h bridges using carrier phase shifted sine PWM technique is implemented in MATLAB/Simulink platform and merits of the proposed inverter system is verified through experiments based on simulations.

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