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DESIGN OF FIR FILTER USING DIFFERENT MULTIPLIER ARCHITECTURE FOR HIGH SPEED AND LOW POWER APPLICATIONS

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Abstract- Finite impulse response (FIR) filter is one of the key components in any DSP and communication systems. The output from the DSP processor is based on the FIR filter performance, so need an efficient FIR filter design, to achieve an efficient output. FIR Filter architecture contains many components; one of the key components is multiplier. Different types of multipliers are available in the digital circuits, but need an efficient multiplier design to get efficient filters. In the existing Vedic and Wallace tree multiplier was designed and implemented using verilogHDL. Partial products generation and reduction in the Wallace tree multiplier getting more complicated in speed and performance and also multiplier needs more gates to implement the design. To reduce the drawbacks in the existing system, to propose a new efficient multiplier named as Birecoder multiplier. It is one of the best multiplier in the digital circuit design. This multiplier overcomes the existing multiplier drawbacks by using multiplexer circuit. Multiplier is design by verilogHDL, after the design Wallace tree multiplier is compared with Birecoder, and analyzes the performance of the multiplier. Implement the design using Modelsim 6.3c and Xilinx ISE. Finally the designed multipliers are applied into the FIR filter, and show the best filter.

Keywords: FIR Filter, Wallace tree, Vedic, verilogHDL, Birecoder

1. Introduction

Finite-impulse response (FIR) filters play an important role in many communication systems. The variety of tasks such as noise cancellation, matched filtering, interference cancellation, attenuation reduction, channel equalization, etc. Different types of architectures and implementation methods were proposed to improve the performance of filters. The unstoppable growth in multimedia and mobile applications has enlarging the demand for low power digital signal processing and Wireless Communication. One of the most used functions executed in DSP

is Finite Impulse Response (FIR) filtering. FIR filter structures are simplified to minimizing the number of operation like additions, subtractions, shifting; multiplication. In FIR filter order varies the stop band energy of the input signal. Reconfigurable FIR filter structural designs were done for low power applications. Multiplications are important operations in FIR filters. But the weight of the filter is constants. Multipliers play an important role in today's digital signal processing and various other applications. In high performance systems uses addition and multiplication of two binary numbers is fundamental and most often used arithmetic operations. Statics shows that more than 70% instructions in microprocessor and most of DSP algorithms perform addition and multiplication. So, these operations overcome the execution time. That's why; there is need of high speed multiplier. The demand of high speed processing has been increasing as a result of expanding computer and signal processing applications. Low power consumption is also an important issue in multiplier design. To reduce significant power consumption it is good to reduce the number of operation thereby reducing dynamic power which is a major part of total power consumption so the need of high speed and low power multiplier has increased. Designer mainly concentrates on high speed and low power efficient circuit design.

2. Related Works

Low power consumption is also an important issue in multiplier design. To reduce significant power consumption it is good to reduce the number of operation thereby reducing dynamic power which is a major part of total power consumption so the need of high speed and low power multiplier has increased. Designer mainly concentrates on high speed and low power efficient circuit design. The objective of a good multiplier is to provide a physically packed together, high speed and low power consumption unit. In this paper first we describe different types of multipliers: Booth multiplier, Sequential multiplier, combinational multiplier, Wallace tree multiplier.

Digital signal processing algorithms spend most of their time multiplying; digital signal processor designers sacrifice a lot of chip area in order to make the multiply as fast as possible; a single-cyclemultiply–accumulate unit often used up most of the chip area of early DSPs. The construction of most digital systems is a large task. Disciplined designers in any field will subdivide the original task into manageable subunits building blocks and will use the standard subunits wherever possible. In digital hardware, the building blocks have such names as adders, registers, and multiplexers.

J. Chen, and W. Ding have been proposed the concept of low Power digital FIR Filter based on low power multipliers and adders. This proposed method includes low power multiplier, serial adder, booth multiplier, and shift and add multipliers, folding transformation in linear phase architecture and applied to fir filters to power consumption. When the filter order is fixed and not changed for particular applications, and filter performance can be made using the

proposed architecture. The power savings is up to 40.3% with minor degradation, and the area overhead of the proposed scheme is less than 4.9%. Booth multiplier, Sequential multiplier, combinational multiplier, Wallace tree multiplier.

3. Partial Products Generation Stage In Wallace Tree Multiplier

Partial product generation is initial step in any binary multiplier. These values are generated intermediately based on the value of multiplicand and multiplier. If the value of multiplier bit is '0', then partial product row is simply zero, and if it is '1', the multiplicand will be copied as it is. From the 2nd bit of multiplication, each partial product row value is shifted left one unit. Partial product generators are done only by using of a series of logic AND gates.

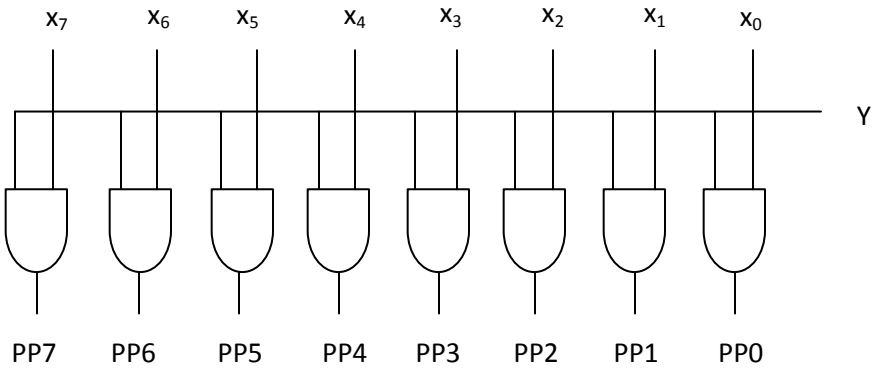

Figure. 1 Partial Products Generation Stage in Wallace tree multiplier

Figure shows partial product generation of Wallace multiplier. The most important operation in the process of multiplication is addition of the partial products which was produced. Performance of the multiplier mainly depends on the performance of the adder.

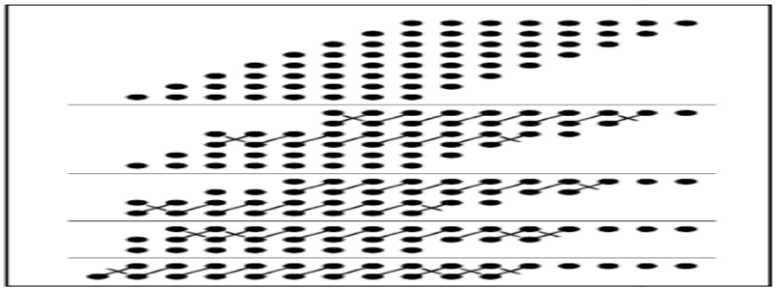

Figure. 2 Wallace Tree Reductions

The above figure determines the dotted notation of Wallace tree reduction. In the step by step reduction are done by using half adders and full adders. After the reduction, finally the bits are added using efficient adder named as SQRT CSLA. It provides better performance for overall multiplier design.

4. Partial Products Generation In Birecoder Multiplier

Partial Products generation and reduction in the multiplier is totally differing from the Wallace tree multiplier. Here multiplexer is used to generate the partial products instead of using AND gate. This process uses four 2:1 multiplexer to perform an 8- bit multiplication operation. In order to perform a 16-bit multiplication need eight 2:1 multiplexer or four 4:1 multiplexer. Depend on the operand bits, number of multiplexer used in the circuit is changed. Partial product generation is initial step in binary multiplier. These values are intermediate values which are generated based on the value of multiplicand and multiplier.

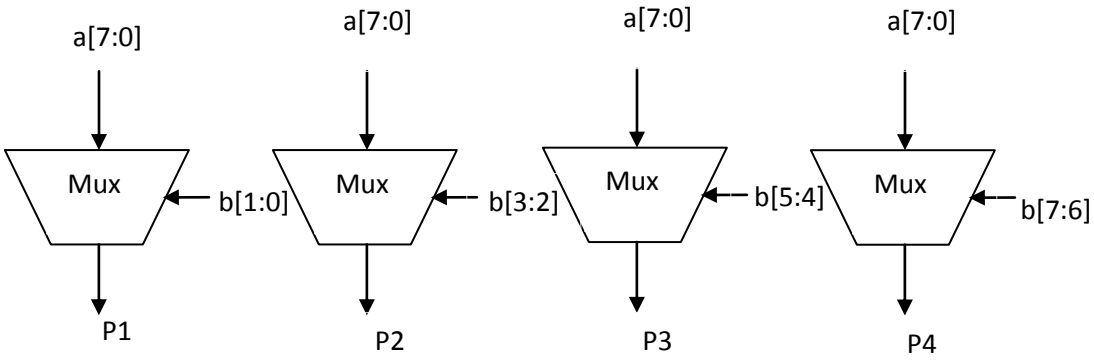

Figure. 3 Partial Products Generation of Bi-Recoder Multiplier

Multiplicand value is directly given to one of the input of 2:1 Multiplexer and N-bit of zero's are given to another input of 2:1 Multiplexer. Multiplier value is given to the selection line of multiplexer value. For instance, 8- bit multiplier requires 8 multiplexer to provide the partial product results. In every stage, single bit of multiplier is considered as selection input of Multiplexer. If it is zero, Multiplexer simply passes '0' to output else if it is one, Multiplexer passes the multiplicand value to output. In this paper, Multiplexer based partial product generation technique considered as a basement tutorial for designing a novel Birecoder multiplier. In every stage of Bi-Recoder multiplier, two bits of multiplier value are considered as selection input. If it is '00' means, Multiplexer simply passes'0' to output else if it is '01' means, Multiplexer passes the multiplicand value to output else if it is '10' means, Multiplexer passes the 1- bit left shifted value of multiplicand to output else it is '11' means, Multiplexer passes the addition value of multiplicand and 1-bit left shifted value of multiplicand to output. In this way,

Bi-Recoder multiplier produces the partial product values effectively. For instance, 8-bit multiplier requires only 4 multiplexer to provide partial product generation. Hence, hardware complexity of Bi- Recoder multiplier reduces effectively. Therefore, an area efficient and low power adder structure also required to increase the performance of Bi- Recoder multiplier. Reduced complexity SQRT CSLA adder is designed in this paper to increase the performance of novelty of Bi-Recoder multiplier.

5. Filter Architecture

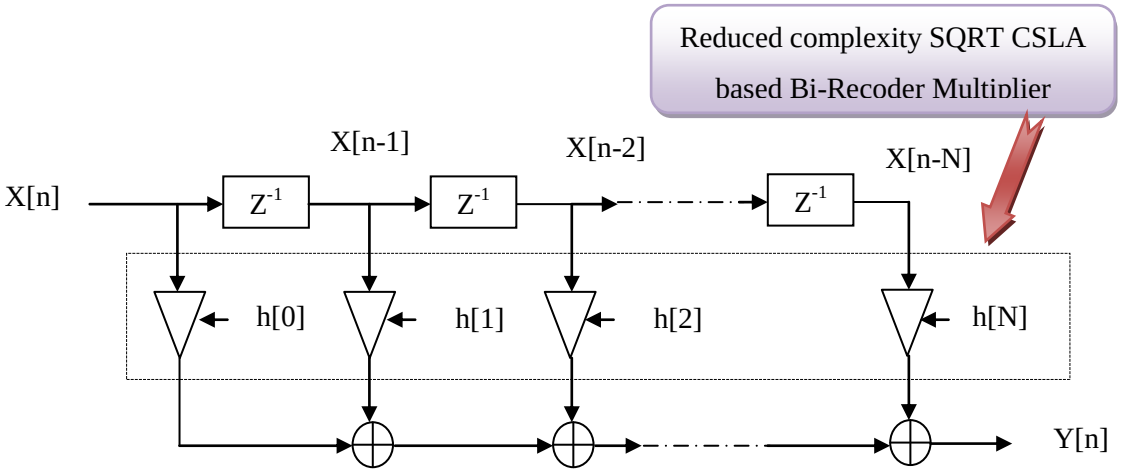

Figure. 4 Design of FIR Filter Architecture

Finite Impulse Response (FIR) filter is used to filter the noise/unwanted signals at finite impulse durations. Multiplication and Accumulation (MAC) unit estimates the duration of periodic impulses. Therefore, high performance of multiplication and accumulation architectures is required to improve the performance of digital FIR filter. SQRT CSLA based Bi-Recoder multiplier is incorporated into multiplication of direct form FIR filter. Hence, absolutely we can improve the performance of digital FIR filter than other best existing FIR filters.

6. Result and Discussion

Simulation was done by using the ModelSim XE III 6.3c simulator. Parameters like area delay and power can be analyzed by using Xilinx ISE 10.1 simulator. Output of the Vedic multiplier is same as other multiplier, compared to the other multiplier speed and accuracy of the Vedic multiplier is higher. The result is shown in the figure. 5 contains different combination of inputs, based on the input it produced the output.

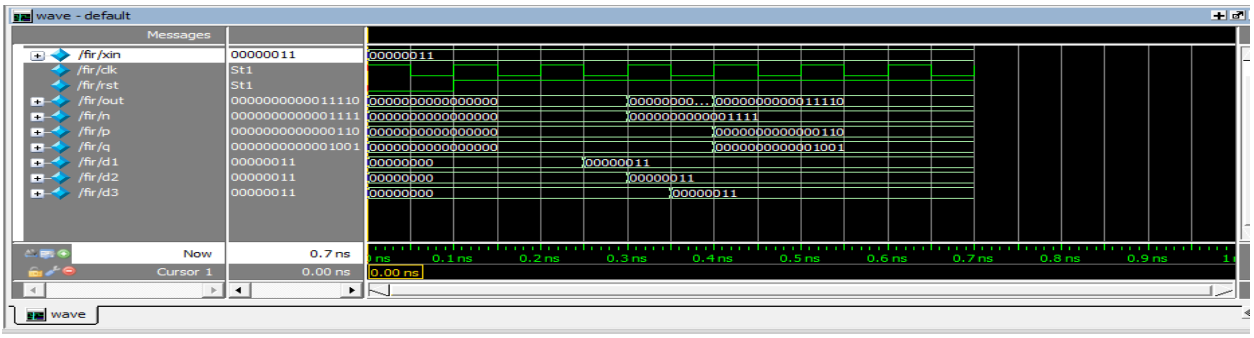

Figure. 5 Simulation Output

6.1 Performance Evaluation

Parameters	FIR Filter Using Wallace tree multiplier	FIR Filter using Bi-Recoder multiplier
LUTs	89	67
Slices	87	46
Delay (ns)	4.644ns	4.357ns
Power (W)	0.252w	0.219w

Table No.1 Comparison of Existing and Proposed Methods

The above table clearly shows difference between the existing and proposed filters. Parameters like LUTs, Slices, Power and delay are varied. Power and delay should be decreased when compared to existing methodology. Speed also increased in the proposed method. It takes less number of hardware compared to the Wallace tree multiplier circuit.

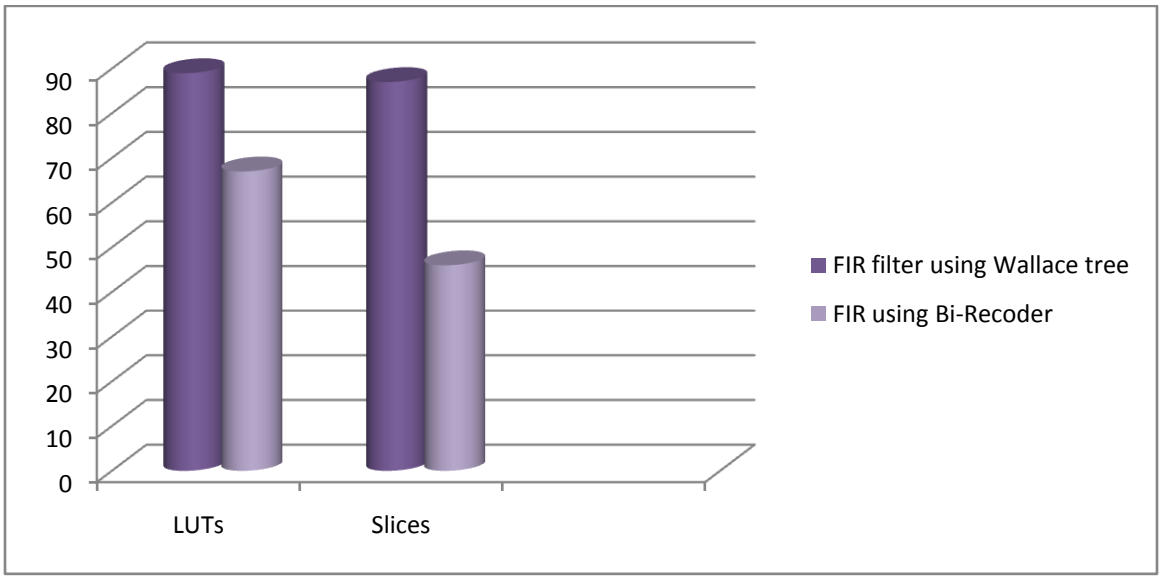

Figure. 6 Hardware Utilization

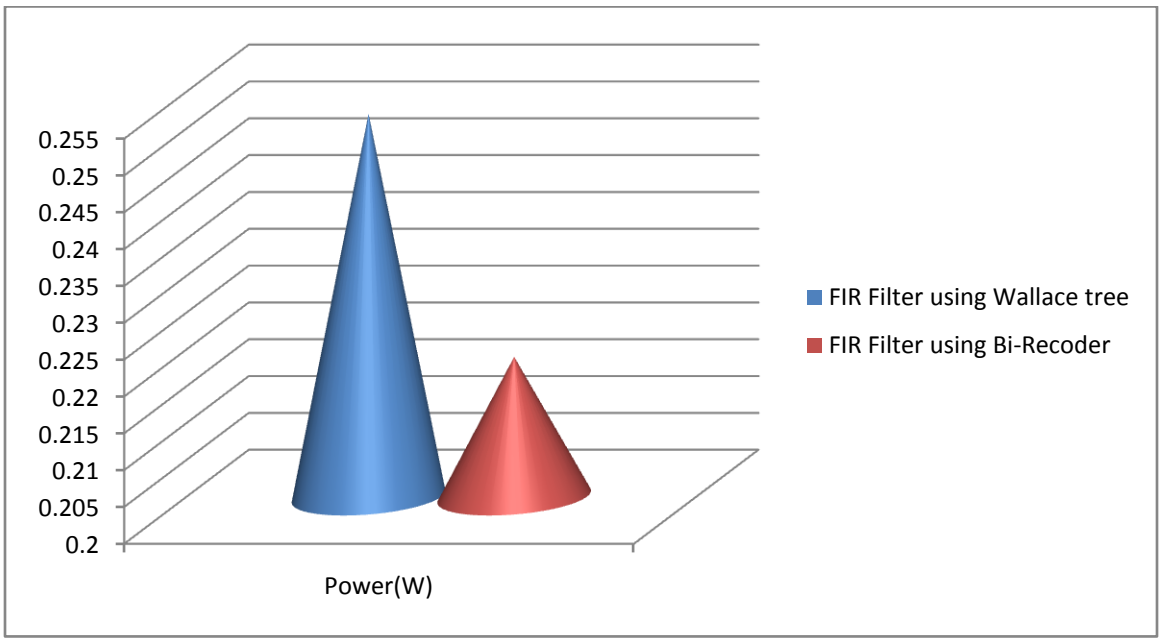

Figure. 7 Delays

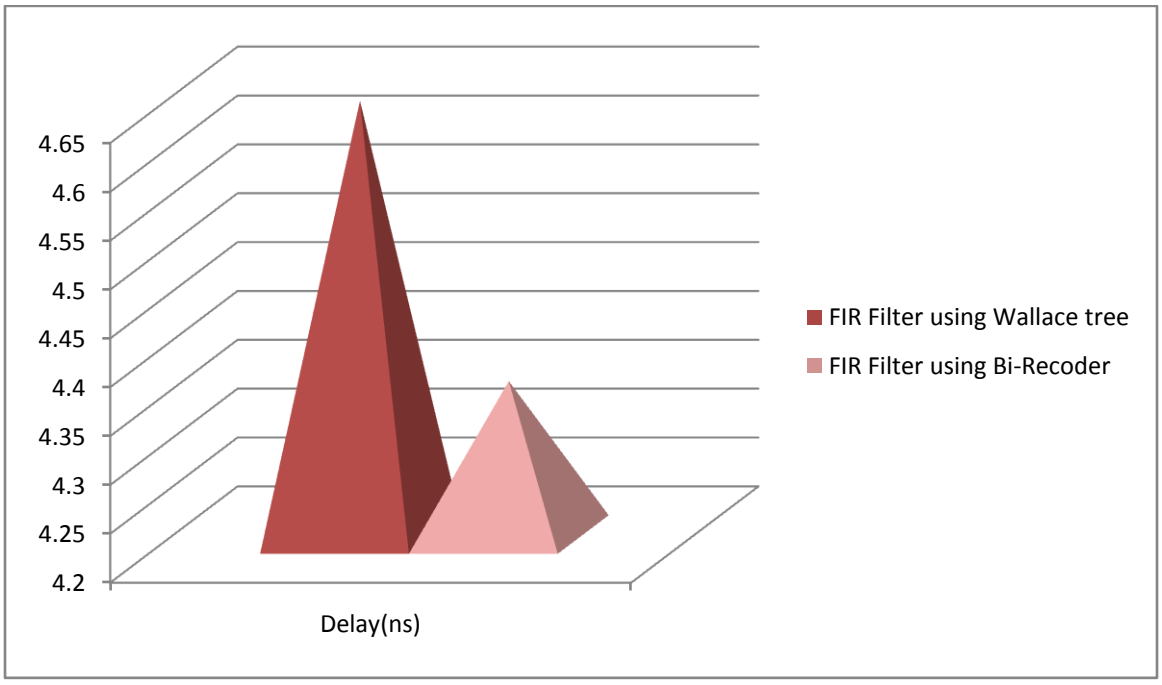

Figure. 8 Power

7. Conclusion

An area efficient, high speed and low power multiplier named as Birecoder multiplier was designed by using the verilogHDL. It reduces the area complexity, latency and high power dissipation in the digital circuits. The proposed multiplier was applied to the direct form FIR filter for verifying the filter operation. After applying the multiplier into the filter, the performance is evaluated. It provides the better results when compared to the other FIR filters used the ordinary MAC. Now the filter is applicable for much application like digital signal processing, wireless communication, image processing etc. The modified FIR filter is suitable for all kind of applications.

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