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A Review of Different Multipliers in Digital Circuits

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Abstract - Multiplication is one of the basic functions in all digital circuits. It is widely used in digital signal processing (DSP) applications. Hardware resources utilization and processing time required by it are more than addition and subtraction. There are two different kinds of multiplication algorithms known as, serial multiplication algorithms and parallel multiplication algorithm. Serial multiplication schemes are widely used in sequential circuits, it contain feedback loop. Parallel multiplication algorithms often used in combinational circuits, it does not contain feedback structures. This paper presents various multiplier architectures. Multiplier architectures generally classified into two categories, one is "tree" multipliers and another one is "array" multipliers. Tree multipliers add as many partial products in parallel as possible and therefore, are very high performance architectures. Multiplication operation involves generation of partial products and their accumulation. The speed of multiplication can be increased by reducing the number of partial products.

Keywords - Serial and parallel multiplier, array multiplier, tree multiplier

1. Introduction

Multipliers play an important role in today's digital signal processing and various other applications. In high performance systems uses addition and multiplication of two binary numbers is fundamental and most often used arithmetic operations. Statics shows that more than 70% instructions in microprocessor and most of DSP algorithms perform addition and multiplication. So, these operations overcome the execution time. That's why; there is need of high speed multiplier. The demand of high speed processing has been increasing as a result of expanding computer and signal processing applications. Low power consumption is also an important issue in multiplier design. To reduce significant power consumption it is good to reduce the number of operation thereby reducing dynamic power which is a major part of total power consumption so the need of high speed and low power multiplier has increased. Designer mainly concentrates on high speed and low power efficient circuit design. The aim of a good multiplier is to provide a physically packed together, high speed and low power consumption unit. In this paper first describe different types of multipliers: Booth multiplier, Sequential multiplier, combinational multiplier, Wallace tree multiplier, Vedic multiplier etc. In next section we will discuss different techniques used in MAC for efficient operations.

2. Related Works

Low power consumption is also an important issue in multiplier design. To reduce significant power consumption it is good to reduce the number of operation thereby reducing dynamic power which is a major part of total power consumption so the need of high speed and low power multiplier has increased. Designer mainly concentrates on high speed and low power efficient circuit design. The objective of a good multiplier is to provide a physically packed together, high speed and low power consumption unit. In this paper first we describe different types of multipliers: Booth multiplier, Sequential multiplier, combinational multiplier, Wallace tree multiplier.

Digital signal processing algorithms spend most of their time multiplying; digital signal processor designers sacrifice a lot of chip area in order to make the multiply as fast as possible; a single-cyclemultiply–accumulate unit often used up most of the chip area of early DSPs. The construction of most digital systems is a large task. Disciplined designers in any field will subdivide the original task into manageable subunits building blocks and will use the standard subunits wherever possible. In digital hardware, the building blocks have such names as adders, registers, and multiplexers.

3. Digital Multipliers

A binary multiplier is an electronic circuit used in digital electronics, such as a computer, to multiply two binary numbers. It is built using binary adders. There are different types of multipliers. Some of these are

1. Array Multipliers
2. Tree Multipliers

Array Multipliers

This multiplier can be classified into following categories:

- Braun Multiplier
- Booth Multiplier
- Modified Booth Multiplier
- Baugh -Wooley Multiplier

Braun Multiplier

Braun Array multiplier is well known due to its regular structure. It is a simple parallel multiplier that is commonly called as carry save array multiplier. This multiplier is avoiding to performing multiplication of two unsigned numbers. It consists of array of AND gates and

adders arranged in iterative structure that does not require logic registers. This is also known as the non-additive multiplier since it does not add an additional operand to result of multiplication. This multiplier is regular in structure, small size, easy to layout and also the design is pipelined in nature. One of the drawback is hardware is underutilized.

Booth Multiplier

Conventional array multipliers, like the Braun multiplier and Baugh Woolley multiplier achieve comparatively good performance but they require large area of silicon, unlike the add-shift algorithms, which require less hardware and exhibit poorer performance. The Booth multiplier makes use of Booth encoding algorithm in order to reduce the number of partial products by considering two bits of the multiplier at a time, thereby achieving a speed advantage over other multiplier architectures. This algorithm is valid for both signed and unsigned numbers. It accepts the number in 2'scomplement form, based on radix-2 computation.

Modified Booth Multipliers

The modified Booth encoding (MBE), or modified Booth's algorithm. The recoding method is widely used to generate the partial products for implementation of large parallel multipliers, which adopts the parallel encoding scheme. The original version of Booth algorithm (Radix-2) had two drawbacks: The number of add subtract operations and the number of shift operations becomes variable and becomes inconvenient in designing parallel multipliers. The algorithm becomes inefficient when there are isolated 1"s. These problems can be overcome by modified Booth algorithm. MBA process three bits at a time during recoding. Recoding the multiplier in higher radix is a powerful way to speed up standard Booth multiplication algorithm.

Tree Multiplier

The tree multiplication algorithm can reduce the number of partial products by employing multiple input compressors capable of accumulating several partial products concurrently. Tree multiplier can handle the multiplication process for large operands. This is achieved by minimizing the number of partial product bits in a fast and efficient way by means of a CSA tree constructed from 1-bit full adders.

Wallace Tree Multiplier

A Wallace multiplier is a parallel multiplier which performs the array multiplication effectively. Array multiplier has more number of gates to perform multiplication. Hence, it occupies large area for computation. In order to overcome this problem, Wallace multiplier with proposed SQRT CSLA is designed. Fig 6 shows reduced complexity Wallace multiplier structure. The reduced complexity Wallace multiplier consists of reduced number of half adders when compared to the conventional Wallace multiplier. In the modified circuit, N^2 AND gates

form the partial products and they are arranged in an inverted triangle order. The matrix is divided into three row groups in the reduced complexity Wallace multiplier.

1) Full adder is used for adding three bits.

2) Single bit and a group of two bits are moved to the next stage directly.

In the final stage of Wallace multiplier, proposed SQRT CSLA is used instead of conventional SQRT CSLA for addition process. It reduces area as well as power.

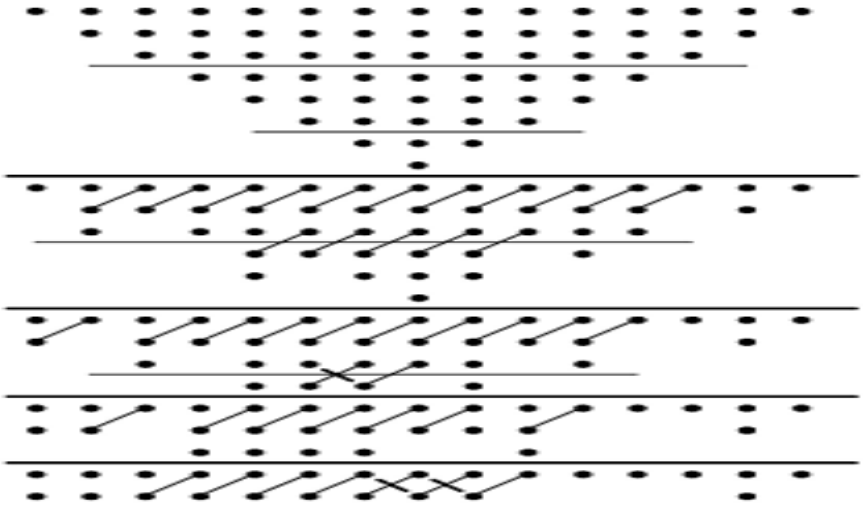

Figure.1 Structure of Wallace Tree Multiplier

Vedic Multiplier

Multiplication is one of the important arithmetic operation in signal processing applications. Signal processing involves multiplication, speed and accuracy is the main constraint in the multiplication process. Speed can be achieved by reducing the computation process in the multiplication technique. Vedic multiplier is efficient multiplication technique. The efficient Vedic multiplication technique is used. The 8-bit Vedic multiplier is designed by using four 4x4 Vedic multiplier and square root carry select adder (SQRT-CSLA). The 8-bit input sequence is divided into two 4-bit numbers. Input to the 4-bit multiplier are a[7:4] & b[7:4], a[3:0] & b[7:4], a[7:4] & b[3:0], a[3:0] & b[3:0]. Intermediate partial products output are added using the three modified adder, named as SQRT-CSLA.

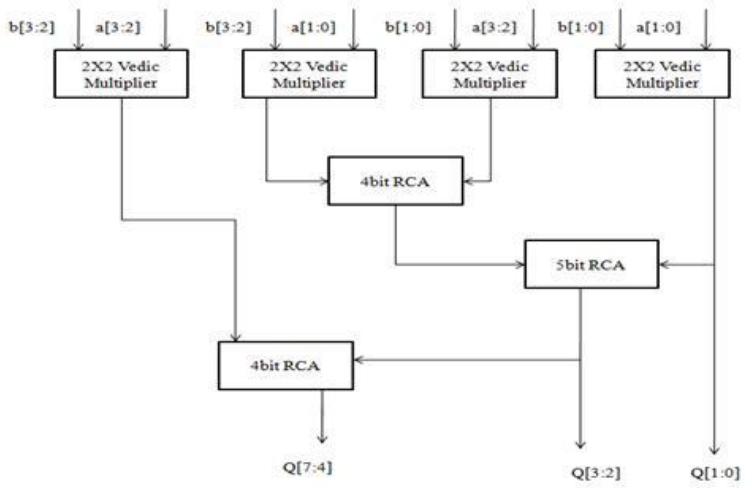

Figure.2 Structure of Vedic Multiplier

4. Comparison

Comparison between different multipliers is done by using various parameters:

Type	Speed	Complexity	Layout	Area
Array	Low	Simple	Regular	Small
Booth	High	Complex	Irregular	Medium
Modified Booth	High	Medium	Irregular	Large
Wallace tree	Very High	More Complex	More Irregular	Very Large
Vedic	Very High	More Complex	More Irregular	Very Large

Table No.1 Comparison of Different Multipliers

5. Conclusion

This paper clearly explains the various performances of the multipliers. Two different category of multiplier is presented in this paper; both the category clearly shows the various

performance measures. The analyzed parameters are speed, complexity, layout and area. These parameters varying depend on the multiplier. Based on the analyzes choose the best multiplier for various applications.

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