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Schematic Design and Spice Synthesis of the Arithmetical Operation

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Abstract: In this work, the analysis of hybrid full adder circuit is designed by using Complementary Metal-oxide semiconductor (CMOS) devices. The adder is one of the most required arithmetical functions of the various digital circuits. Full adder is used to perform the three-bit additions of the given inputs. There are various CMOS logic styles are used to build the full adder circuit. In this work, the hybrid full adder is designed by using the transmission gate logic by using CMOS devices. Voltage scaling and reduced transistor size are features of the conventional CMOS architecture. Complementary pass transistor logic (CPL) is another type of logic used to build an adder. The CPL design isn't appropriate for low-power applications. The proposed circuit is implemented by using S- edit in Tanner EDA. The proposed circuit performances are evaluated by using T-spice in Tanner EDA. The proposed full adder is efficiently used for the Arithmetic and logic unit (ALU).

Keywords: Metal-Oxide-Semiconductor (MOS), Full adder (FA), Schematic Editor, Tanner, CMOS.

1. Introduction

Full adder operation is required blocks in the field of the microprocessors. One of the most important areas of research in VLSI system design is the construction of area and power efficient high speed data path logic systems. The time required to propagate a carry through a digital adder limits the speed of addition. In a basic adder, the sum for each bit location is created sequentially only after the preceding bit position has been summed and a carry propagated into the next place. The CLSA is utilized in many computing systems to solve the problem of carry propagation delay by generating numerous carries separately and then selecting one to create the total. There is various logic styles are used for the design of full adder circuit. That is, transmission gate logic, static CMOS logic and so on. By using these logic styles, the full adder is performed with the reduced number of transistors counts as well as delay [1]. In VLSI design environment, the number of transistors counts and delay is one of the main considerations for chip implementation [2]. Static CMOS design is providing some advantages like simplicity and power consumption but in the field of the chip design the area requirement is somewhat higher

compare than the dynamic design [3]. In general, the standard CMOS design has voltage scaling and minimized transistor sizing. Complementary pass transistor logic (CPL) is also one of the logic to construct the adder design [4]. CPL design is not applicable for the low power applications. Several logic style based adder design is used for various digital circuits like NAND-NOR cells, Multiplier, Multiplication and accumulation (MAC), Dividers [5]. In this work, the hybrid logic based full adder is implemented to provide the minimum number of transistor counts and power utilizations [6].

2. Proposed Design Based Hybrid CMOS Logic

The X-or gate is mainly used to construct the full adder in X-OR based full adder. The new proposed design is implemented by using three logic [7]. Proposed method presented the high-speed CMOS circuit's full adder for embedded system applications. That is, pass transistor logic and static CMOS logic [8]. The proposed design is not only applicable for high-speed applications, it also suitable for the high driving capability [9]. By using this logic, the numbers of transistor counts are highly reduced compare than the traditional logic style [15]. The only drawback of the design is power utilizations [10].

2.1 Adder Specialization

The full adder circuit is performed based on the three categories. The sum and carry generations is mathematically expressed ad below.

$$Sum = X \oplus Y \oplus Z_{in}$$

$$Carry = X.\ Y + Z_{in}\ .(X \oplus Y)$$

The full adder circuit is implemented by using three main catagories are listed below.

2.1.1 Full Adder by Using XOR Logic:

where P is $X \oplus Y$ and P' is the complement of P.

$$Sum = X \oplus Y \oplus Z_{in} = P \oplus Z_{in}$$

$$Carry = Z\ .P' + Z_{in.}\ P$$

2.1.2. Full Adder by Using XNOR Logic:

The mathematical expression of XNOR logic based full adder is expressed as below,

$$Sum = \overline{\overline{(X \oplus Y)} \oplus Zin}$$

$$= \overline{P' \oplus Zin}$$

$$\text{Carry} = X.\ P' + Z_{in.}\ P$$

C. Generalized Full Adder Logic*:*

The logic of the full adder is given in the following expression.

$$\text{Sum} = P \oplus Z_{in} = P.\ Z'_{in} + P'.\ Z_{in}$$

$$\text{Carry} = X.\ P' + Z_{in.}\ P$$

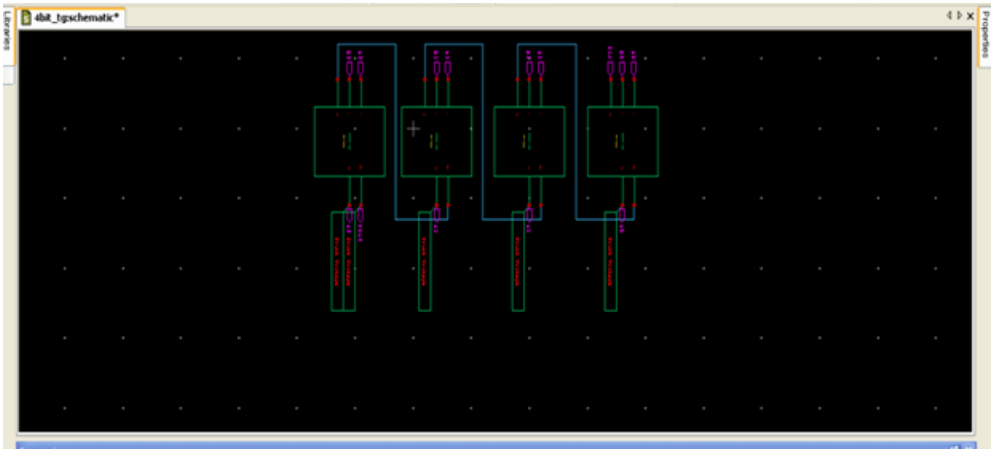

Figure 1: Schematic design of the proposed full adder

It stated the efficient full adder-based hybrid CMOS logic style [11]. Pass logic is one of the efficient logics to build the full adder in terms of the transistor counts [12]. The proposed logic style is providing the minimum number of transistor count utilizations as well as the power consumption [13]. Pass logic based full adder circuit is applicable of high-speed applications [14].

3. Results and Discussions

The proposed hybrid full adder circuit is implemented by using Tanner EDA tool by using CMOS technologies. In general, voltage scaling and transistor sizing are reduced in conventional CMOS designs. Complementary pass transistor logic is also used to build the adder architecture. The CPL design is inapplicable to low-power applications. Several logic type adder designs are utilised in various digital circuits such as NAND-NOR cells, multipliers, multiplication and accumulation, and dividers. The hybrid logic-based full adder is built in this study to give the fewest number of transistors counts and power utilizations.

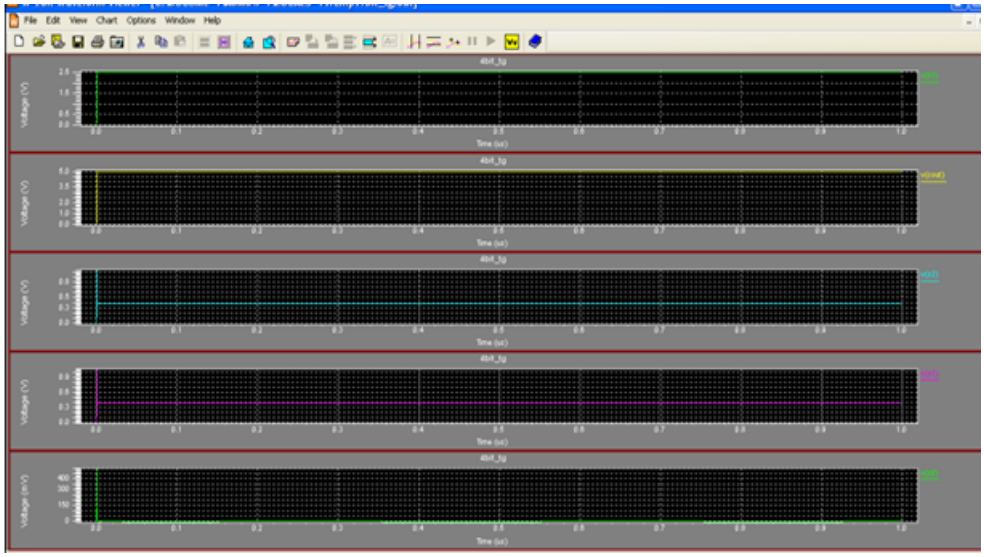

Figure 2: W-Edit waveform for the proposed full adder design

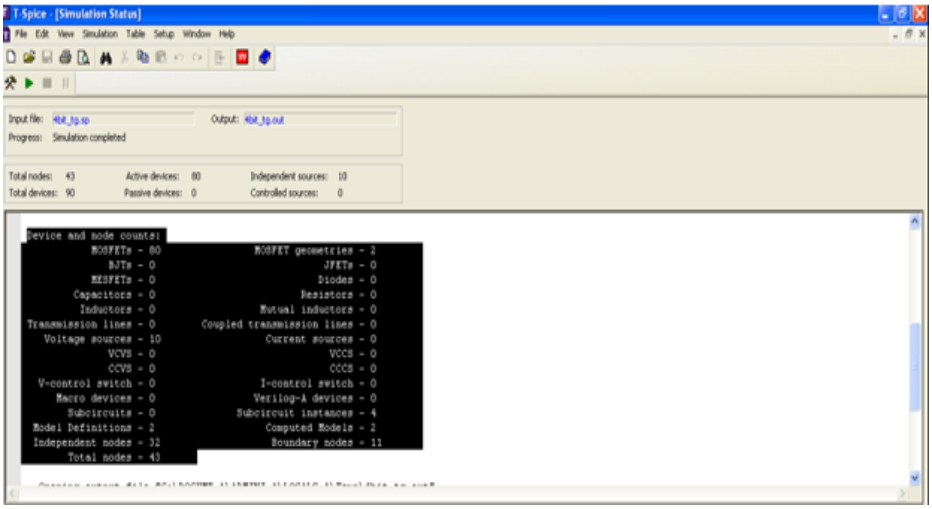

Figure 3: Synthesis results of number of transistor counts utilization

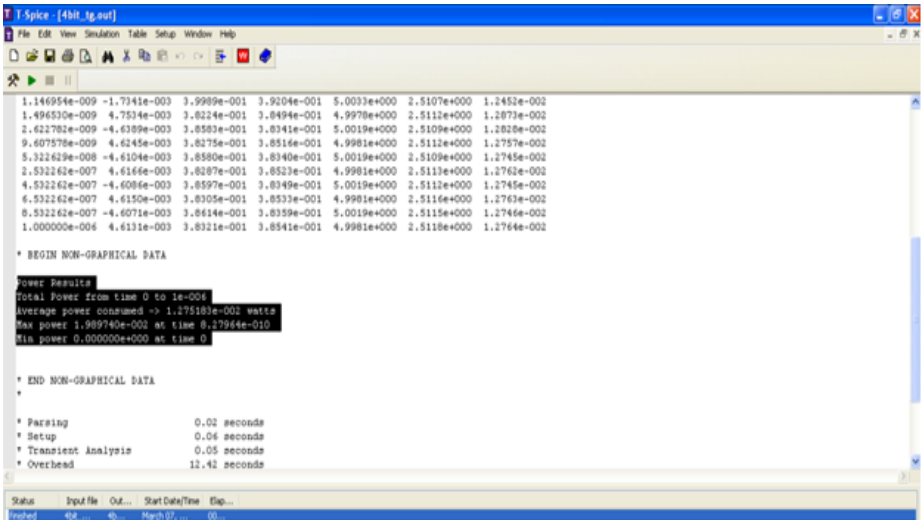

Figure 4: Synthesis Power results for proposed adder

The proposed design technology is 250 nm CMOS technology. The hybrid CMOS logic design is providing efficient addition function with the minimum number of transistors counts as well as power consumption Figure 1. The output waveform of the proposed work was carried out by using W-Edit and it is shown in Figure 2. The simulation of the proposed full adder was estimated by using T-spice. The synthesis results are illustrated in Figure 3 and Figure 4.

4. Conclusion

In this work, the hybrid CMOS logic based full adder is implemented by using Tanner EDA tool in terms of the VLSI design environment. The adder is one of the most often used arithmetic functions in digital circuits. The three-bit additions of the provided inputs are performed using a full adder. The entire adder circuit is built using a variety of CMOS logic designs. The hybrid full adder is constructed in this paper utilising transmission gate logic and CMOS components. The traditional CMOS architecture includes voltage scaling and smaller transistors. The proposed work performance is efficient compared than the other logic technologies like CMOS, CPL, and TGA. The proposed work is mainly applicable for the Arithmetic and logic unit (ALU) and microprocessors. The transistor sizing is one of the main considerations for the chip implementations. In future, the nanometer is optimized to reduce the length and width of the PMOS and NMOS transistors.

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