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Pipelined FFT Architecture Using Single Path Delay Feedback Structure

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Abstract: In general, FFT architecture is used to convert time domain signal into frequency domain signal. In all transmitter and receiver FFT/IFFT is one of the main process to get a efficient transmission of information. Pipelined FFT provide better computation than compared to parallel FFT. Radix-2 FFT structure is used to compute the 64-point FFT architecture. Single path delay feedback method is used for reduction of butterfly structure. SDF structure provides fast computation than other structures. Radix-2 takes more time to perform the operation, and also it takes more complex multiplier for twiddle factor multiplication. Radix-4 is the improved version of radix-2; it reduces the stages of butterfly operation. Butterfly structures are used to determine frequency response of time domain signals in IFFT and to determine timing response in frequency domain signals. FFT processors can be classified as two categories, as Decimation in Time (DIT) FFT and Decimation in Frequency (DIF) FFT. The Radix-2 structure with SDF is simulated using Modelsim simulator.

Keywords: Radix-2, FFT, SDF, SDC, FPGA

1. Introduction

VLSI based Fast Fourier Transform (FFT) and Inverse Fast Fourier Transforms (IFFT) is the two important processes in many communication systems [1]. Today pipelined FFT process is widely used because of speed. Parallel FFT processor occurs delay during the computation and the code is also complex in nature [2]. So, to avoid this drawback pipelined FFT processor is used. Fast Fourier Transformation (FFT) is one of the digital signal processing operations used for frequency transformation [3]. In nature, IFFT is used to analyze the frequency characteristics of discrete time domain signals. On the other hand, FFT is used to analyze the timing characteristics of discrete frequency response [4]. Butterfly structures are used to determine frequency response of time domain signals in IFFT and to determine timing response in frequency domain signals [5]. FFT processors can be classified as two categories, as Decimation in Time (DIT) FFT and Decimation in Frequency (DIF) FFT. Most of the cases, DIT algorithm is using for the FFT computation in the communication system [6]. The communication field FFT.

Different types of radix algorithms are used in the FFT processor. The performance of the FFT varies with different radix algorithm. Power consumption, hardware cost and memory requirement of each radix is varied in the FFT processor. Radix-2 FFT algorithm is an efficient method for computing the Discrete Fourier transforms [7]. It uses cooley-Tukey algorithm for simplify the butterfly structure.

The implementation of 64-point FFT/IFFT is using radix-8 algorithm. VLSI implementation of pipelined FFT architecture has three main concerns; these are high speed, low power consumption, and reduced chip area [8]. OFDM system is one of the important applications of FFT and IFFT processor [9]. Memory is one of the major elements in the processor, to eliminate the Read only memories used to store the twiddle factor values [10]. To avoid this problem, reconfigurable complex multiplier achieves a less ROM usage for FFT and IFFT processor, and also it reduces the truncation error [11].

2. Proposed Radix-2 Butterfly Structure

Radix-2 takes more time to perform the operation, and also it takes more complex multiplier for twiddle factor multiplication [12]. Radix-4 is the improved version of radix-2; it reduces the stages of butterfly operation [13]. It improving the speed and reducing the computational cost of the processor [14]. It also reduces many complex multiplication operations in the Butterfly.Radix-2 Single-path Delay Feedback (R2SDF) FFT is a parallel technique for estimating the frequency response of discrete timing response [15]. This structure also referred as "stream-like" processing of block-based algorithm. One of the key advantages of Radix-2 FFT is processing the data in a parallel manner whenever input points are available. Radix-2 Butterfly structure is shown in Figure1.

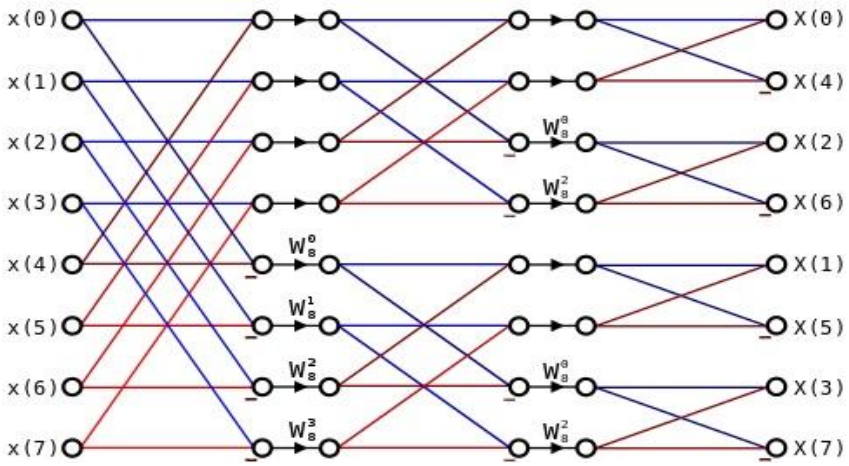

Figure 1: Radix-2 Butterfly Structure

Single Path Delay Feedback (SDF)

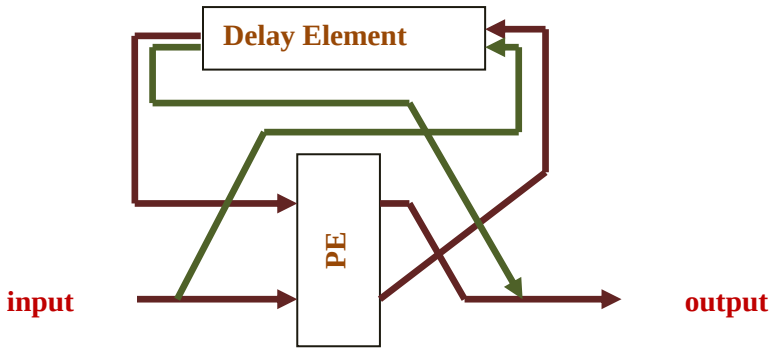

Figure 2: Basic Structure of SDF

Single path delay feedback (SDF) method is used to achieve the speed of the FFT processor (Figure 2). The SDF structure uses delay element to get the output response of the FFT. One of the main advantages is speed of the processor is get increased, but does not concentrate the power and area utilization. So, the only drawback is power consumption of the circuit during the computation of FFT architecture.

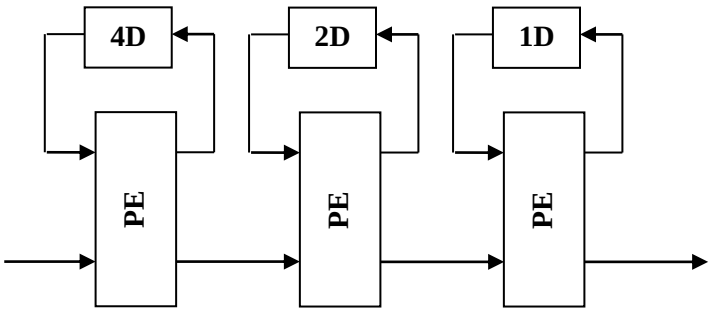

Figure 3: Radix-2 8-point FFT Structure

The input data sequence is broken down into two parallel data streams (Figure 3). In each stage of Radix-2 SDF FFT processors, half of the input data is delayed via feedback delay unit and processed with second half of the input data. The delay elements used are 4, 2 and 1 respectively for three stages in 8-point Radix-2SDF FFT processors. Hence, total number of delay elements used is 4+2+1=7 in case of 8-point R2SDF FFT.

3. Results and Discussion

The input data stream is divided into two parallel data streams Figure 3. Radix-2 SDF FFT processors include three stages. Radix-2 takes more time to perform the operation, and also it takes more complex multiplier for twiddle factor multiplication. Radix-4 is the improved version of radix-2; it reduces the stages of butterfly operation. Pipelined FFT provide better computation than compared to parallel FFT. Radix-2 FFT structure is used to compute the 64-point

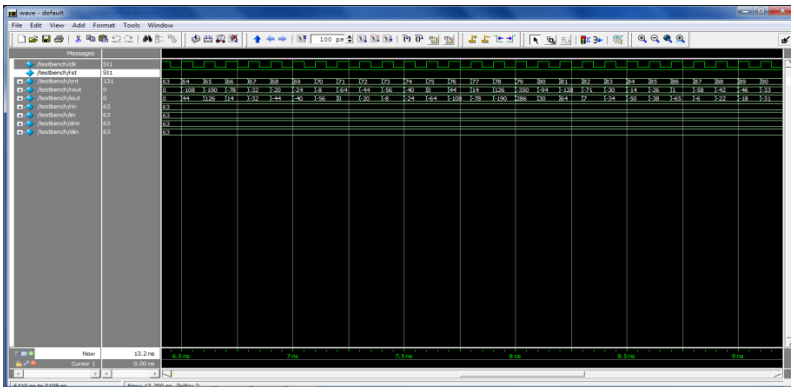

Figure 4: Simulation Output of Radix-2 FFT Structure

Table 1: Comparison between Parallel and Pipelined FFT Structure

Parameters	**Parallel FFT**	**Pipelined FFT**
Delay (ns)	4.21ns	3.01ns
Slices Used	183	150
LUTs Used	265	193
Power (Watts)	4.32	2.18

The simulated output of Radix-2 Pipelined FFT is shown in Figure. 4 and in Table 1. The output can be taken from Modelsim 6.3c simulator. The input and outputis given in the simulation are based on clock signal.

4. Conclusion

In this paper, Radix-2 based pipelined FFT was designed. Radix-2 takes more time to perform the operation, and also it takes more complex multiplier for twiddle factor multiplication. Radix-4 is the improved version of radix-2; it reduces the stages of butterfly operation. Pipelined FFT provide better computation than compared to parallel FFT. Radix-2 FFT structure is used to compute the 64-point FFT architecture. Single path delay feedback method is used for reduction of butterfly structure. Butterfly structures are used to determine frequency response of time domain signals in IFFT and to determine timing response in frequency domain signals. FFT processors can be classified as two categories, as Decimation in Time (DIT) FFT and Decimation in Frequency (DIF) FFT. The designed Pipelined FFT is compared with parallel FFT, the output response of the pipelined FFT provide better results than parallel. The proposed FFT is applied into many applications like OFDM, SDR etc. The results were evaluated and analyzed using Xilinx simulation environment.

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