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Effective Communication Using Adaptive FFT/IFFT

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Abstract: In any communication system FFT/IFFT is one of the important processes to get an efficient output from the communication system. FFT/IFFT is a process used to convert time signal to frequency signal and frequency signal to time signal. Different FFT/IFFT structures are used to process the signal in different way. But one of the drawbacks in the system is using only one FFT/IFFT process at a time. To improve the system efficiency by using adaptive FFT/IFFT, adaptive technique changes the FFT/IFFT structure based on the signal entering into the system. Single Path Delay Feedback (SDF) and Single path Delay Commutator (SDC) are the two-process used in the system. The frequency domain signal is converted into the time domain using the Inverse Fast Fourier Transformation (IFFT). On the transmitter side, IFFT processors are used to transform the frequency signal (which comes from modulation method) into a time signal. FFT is also used to transform a time domain signal (from a channel decoder) into a frequency domain signal. These kinds of process achieve higher efficiency when compared to the previous system.

Keywords: FFT, IFFT, Adaptive, SDF, SDC

1. Introduction

In today's environment, wireless data transmission solutions encounter several problems. Various OFDM models have been created by significant enterprises based on their architecture investigation. To realize the data transmission features of the OFDM system, many sorts of sources such as digital bits, sounds, movies, broad broadcast messages, and command and control signals are explored. Long-distance communications are driven and established using Orthogonal Frequency Division Multiplexing (OFDM) and Software Defined Radio (SDR) technology, which provides cost efficiency, flexibility, and power. Traditionally, it is not possible to transmit timing signal over a long distance. Thus, it is required to design the conversion process of timing signal into frequency signal [1]. Fast Fourier Transformation (FFT)

technique is one of the important frequency transformation techniques in which twiddle factor multiplication performs the conversion process [2]. Twiddle factor is also referred to as rotational factor. In twiddle factor multiplication, the frequency response of corresponding timing signal should be found with the help of amplitude and phase shift of the corresponding signal [3]. In OFDM transmitter, To transform frequency signals into time domain signals, the Inverse Fast Fourier Transformation (IFFT) approach is utilized. Similarly, the Fast Fourier Transform (FFT) approach is employed in the OFDM receiver to transform time domain signals into frequency domain signals [4].

Pipeline technique based FFT technique has been designed and implemented by using clock-based processing element architectures [5]. Two general architectures called SDF and MDC architectures are used widely to convert time domain signal into frequency domain signal [6]. But, in the research work of, a novel architecture called "Radix-2 Single Deep Delay Feedback (R2SD^{2}F)" is designed for performing frequency transformation processes. In the proposed architecture 2*(N/2) and single N delay is used to perform the FFT function. In middle stages, proper commutator and feedback structures are used to getting results in appropriate clock periods [7]. This is one of the best architectures which further can be useful in design of OFDM based wireless data transmission system. The combined architectures are used to perform the frequency transformation processes [8]. Because of dependable advantages in SDF and MDC independently, combined SDC/SDF architectures are used in this research work [9]. In SDC/SDF architecture $\sqrt{n}$ -1 stages of SDF dataflow structure and single SDC stages are used to perform the frequency transformation processes. Radix-r^k method is used in this work make an efficient and reduces the hardware utilization effectively [10]. This is one of the speed frequency transformation based processors than Single or Multi Delay commutator structure. But when compared to Single-path Delay Feedback structure, the performance would leads to poor results [11].

2. Proposed System

The frequency domain signal is converted into the time domain using the Inverse Fast Fourier Transformation (IFFT). On the transmitter side, IFFT processors are utilized to transform the frequency signal (which comes from modulation approach) into a time signal [12]. FFT is also used to transform a time domain signal (which comes from a channel decoder) to a frequency domain signal. FFTs using single path delay feedback (SDF) and single path delay commutator (SDC). In terms of VLSI key issues, each have distinct forms of benefits.

Radix-2 SDF FFT is based on only feedback and single path delay structure. Hence, it has less combinational and sequential delay [13]. Delay performances are measured in terms of Minimum Period (ns), Maximum arrival delay after clock (ns), Maximum arrival delay before clock (ns) and Maximum combinational delay (ns). From the delay sequence, it is clear that R2SDF FFT is the best suitability to high speed & high throughput applications [14]. In other

hand, it uses multiple hardware components in terms of slices and LUTs to perform the signed addition and signed subtraction at each and every successive stages.

Radix-2 SDC FFT is based on commutator structure along with feedback and single path delay structure. Commutator structure in the sense referred as extending the phase shift signal sequentially to reduce the signed addition and signed subtraction-based hardware utilization [15]. Hence, R2SDC FFT utilizes less hardware in terms of Slices (Number of CMOS count) and Look up Tables (LUTs). In other hand, R2SDC FFT architecture has more critical delay (All the delay elements mentioned in previous paragraph) due to critical paths involved in commutator structures. Figure 1. Shows adaptive Fast Fourier Transformation (FFT) processors.

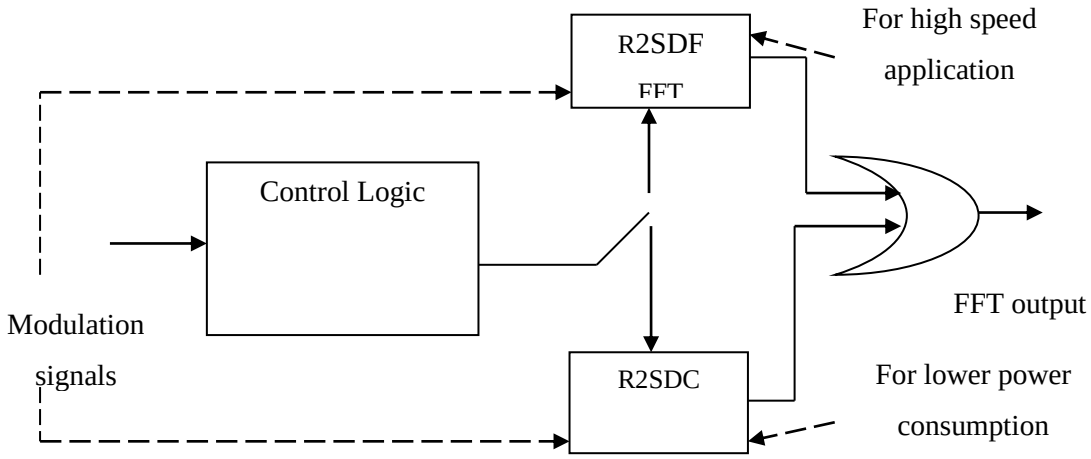

Figure 1. Adaptive FFT Process

In proposed an adaptive FFT model, two efficient pipelines based FFT architectures are used namely SDF and SDC FFT. As discussed earlier, both SDF and SDC FFT have different types of advantages. SDF FFT is better in the perspective of high speed & high throughput functionalities and SDC FFT is better in the perspective of less hardware utilization & lower power consumption.

3. Simulation Results and Discussion

In the current study, ModelSim 6.3C is utilized to test the suggested adaptive model. Figure 2 shows the simulation result of the suggested adaptive FFT model for high-speed requirements. The signal's mode is set to '0' in Figure 2. The width of the input is deemed to be '8-bit'. The output width is also regarded to be '8-bit'.

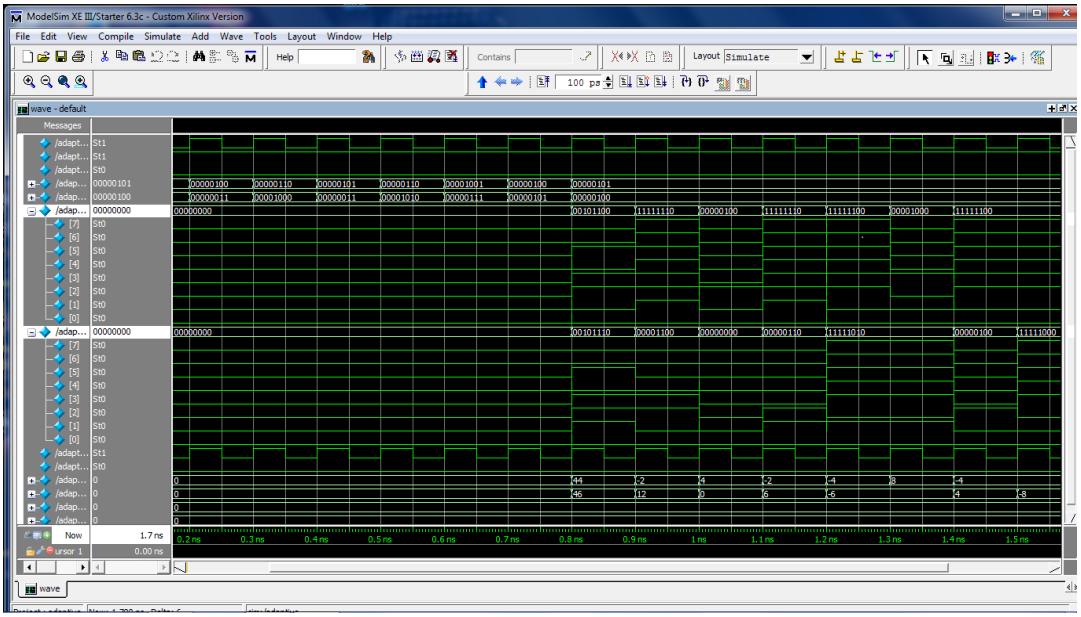

Figure 2: Simulation result of proposed adaptive FFT model for SDF

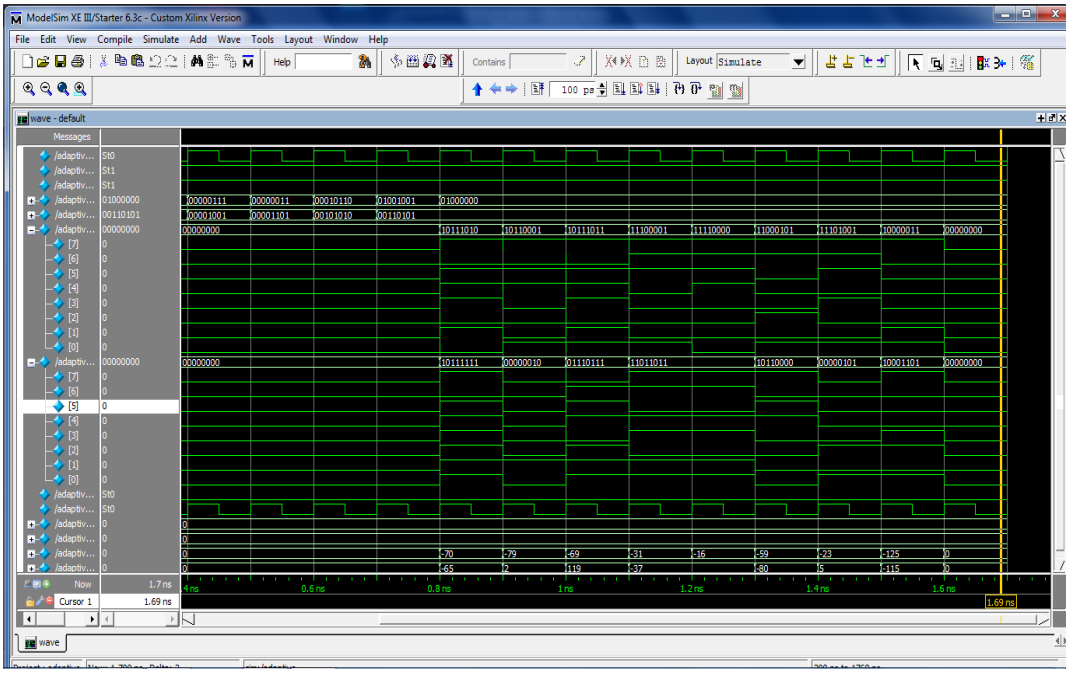

Figure 3: Simulation result of proposed adaptive FFT model for SDC

Table 1: Comparison results of both R2SDF FFT and R2SDC FFT

Type	Slices	LUT	Delay (ns)	Frequency (MHz)	Power (mW)	Application
R2SDF FFT	490	842	20.710	45.042	643	**High Speed**
R2SDC FFT	354	579	23.256	42.183	556	**Low Area and Low Power**

Figure 3 depicts the simulation result of the suggested adaptive FFT model for low area and low power consumption requirements. The proposed adaptive FFT model can be synthesized successfully by using Xilinx 12.1i design tool. The main concerns of VLSI system design environment are reducing the hardware utilization, delay consumption and power consumption.

4. Conclusion

In this work, an adaptive FFT structure is designed by using two effective frequency transformation techniques such as Radix-2 Single path Delay Feedback FFT and Radix-2 Single path Delay Commutator FFT. Adaptive technique changes the FFT/IFFT structure based on the signal entering into the system. Single Path Delay Feedback (SDF) and Single path Delay Commutator (SDC) are the two-process used in the system. The frequency domain signal is converted into the time domain using the Inverse Fast Fourier Transformation (IFFT) on the transmitter side. Verilog Hardware Description Language (Verilog HDL) is used to design an adaptive FFT model. It is a synthesizable language. Hence, the synthesis results of both Radix-2 SDF and Radix-2SDC FFT are compared through Xilinx ISE design tool in Table 1. From the synthesis results, this thesis estimates R2SDC FFT offers 38.41% improvements in hardware slices, 31.23% improvements in LUTs and 13.5% improvements in power consumption than R2SDF FFT.

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