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LOW POWER RADIX-2 BASED SINGLE PATH DELAY FEEDBACK FFT WITH DIF ALGORITHM

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Abstract: In this paper, describe a processor architecture customized to radix-2 based SDF FFT algorithm. The proposed architecture supports all FFT sizes, required by the OFDM applications. The main goal of the proposed architecture is to reduce the area, latency, power and also to decrease computational path for speed up the FFT processor calculation. The proposed low power radix-2 based single path delay feedback FFT architecture with DIF algorithm applies various periodicity properties of twiddle factors multiplier. In other hand, Decimation in Time (DIT) is mostly used to convert the frequency domain signal into time domain signal. The main goal of the VLSI design is to reduce the hardware utilization, delay, and power consumption of the architecture. Generally, SDF architecture is designed for high-speed applications. It offers less delay during the computation of FFT process to implement the processor in 16-point SDF FFT architecture with DIF algorithm. The processor has been synthesized on a Xilinx ISE 12.4design technology and both area efficiency and performance have been evaluated.

Keywords: Fast Fourier Transform, Single Path Delay Feedback (SDF), FFT, Decimation in Frequency (DIF) Algorithm, SDC, IFFT.

1. Introduction

The Fast Fourier Transform (FFT) is a frequency transformation technique used in digital signal processing. IFFT is a technique for analysing the frequency characteristics of discrete time domain signals in nature. The two types of FFT calculations are Decimation in Time (DIT) and Decimation in Frequency (DIF). MIMO-OFDM and Software Defined Radio (SDR) technologies drive and build long-distance communications with cost effectiveness, flexibility, and power [1].

Traditionally, it is not possible to transmit timing signal over a long distance. Thus, it is required to design the conversion process of timing signal into frequency signal [2]. Fast Fourier Transformation (FFT) technique is one of the important frequency transformation techniques in

which twiddle factor multiplication performs the conversion process [3]. Twiddle factor is also referred to as rotational factor [4]. In twiddle factor multiplication, the frequency response of corresponding timing signal should be found with the help of amplitude and phase shift of the corresponding signal [5]. In OFDM transmitter, Inverse Fast Fourier Transformation (IFFT) technique is used to convert frequency signal into time domain signals. Similarly, OFDM receiver has Fast Fourier Transformation (FFT) technique is used to convert time domain signal into frequency domain signals [6].

2. Related Works

Proposed the pipeline based split radix FFT architecture has been developed for improving the combinational and sequential delay [7]. This article presents a full custom one-bit slice delay commutator design for a pipeline split radix FFT (SRFFT) architecture. Pipelining register is added in every input/output block in the proposed FFT structure [8]. Pipelined architecture has AND gated D Flip-flop (DFF). It reduces sequential delay before clock and after clock. Butterfly Unit (BU) or Processing Element (PE) architectures are explained briefly in this article [9].

The Radix-2^3 technique was used to create a 64-point FFT, which was then implemented using the SDF architecture. This method ensures that the RAM and multiplier are fully used [10]. By reducing 64-point FFT into a two-dimensional framework of 8-point FFTs, this approach achieves 64-point FFT. This FFT is broken down into 4-point and 2-point FFTs [11]. To attain quicker computing performance, the complex multiplier employed in this study was created utilizing a modified Booth encoding approach with the aid of the Radix-4 structure.

Bit Parallel Multiplication (BPM) based Pipelined FFT architectures are designed to improve the performances. This paper is mostly concentrated on pipelined architecture and BPM based multiplication architecture [12]. Decimation in Frequency (DIF) FFT is mostly used to convert the time domain signal into frequency domain signal. In other hand, Decimation in Time (DIT) is mostly used to convert the frequency domain signal in to time domain signal. However, in the OFDM wireless transmission system, improvements of receiver side is more important than transmitter side.

In the study of Kumar, A, realization is made on the structure of butterfly to improve the performance of FFT. The structure of butterfly structure consists of real addition, signed complex multiplication and real subtraction processes [13]. In this study, number of complex multipliers and complex adders, Memory size and Control logics are compared for different types of FFT architectures such as R2SDF FFT, Radix-4 SDF (R4SDF) FFT, Radix-4 Single-path Delay Commutator (R4SDC) FFT, Radix-2^2 SDF (R2^2SDF) FFT, Radix-2 Multi-path Delay Commutator (R2MDC) FFT and Radix-4 MDC (R4MDC) FFT [14]. Further this study concludes that Radix-4 structures provide better performance than Radix-2 FFT structures in terms of utilization of complex number of additions and multiplications.

Described the Radix-8 64-point FFT/IFFT algorithm is implemented with the help of fixed width modified booth multiplier. In normal Radix-2 and Radix-8 FFT algorithm, Read Only Memory (ROM) is used to store the twiddle factors. Number of Look up Tables (LUTs) has been increased due to ROM of FFT algorithm [15]. To eliminate the usage of ROM, a reconfigurable complex multiplier named as fixed width modified booth multiplier is designed in this review. Hence, the design of reconfigurable complex multiplier based FFT is named as "ROM-less FFT/IFFT".

3. Structure of DIF FFT

The butterfly structures are generally represented as Radix-2 structures, because of processing the two stages in every time period. In case of 2-point DIT FFT, after the twiddle factor multiplication function only, complex addition and subtraction processes are involved. The frequency representation of discrete time domain signals is constructed using the DIF FFT. DIF FFT, on the other hand, is used to create the time representation of signal frequency representation. We can design 8-point, 16-point, 32 point, and 64-point FFT processors in the same way. Even and odd samples of data transformation in FFT processors are represented by equations (1) and (2). The 8-point Radix-2 DIF FFT structure is also shown in Figure 1. We can easily create Radix-2 DIF FFT processors for various locations, similar to Figure 1. In generalized FFT architecture, a greater number of computational paths is involved to determine the spectrum characteristics of discrete time signals. Due to large number of computational paths, a greater number of logic elements is utilized to design the FFT processors. Also, delay for FFT computation can be increased significantly. To overcome these disadvantages of traditional Radix-2 FFT is preferred.

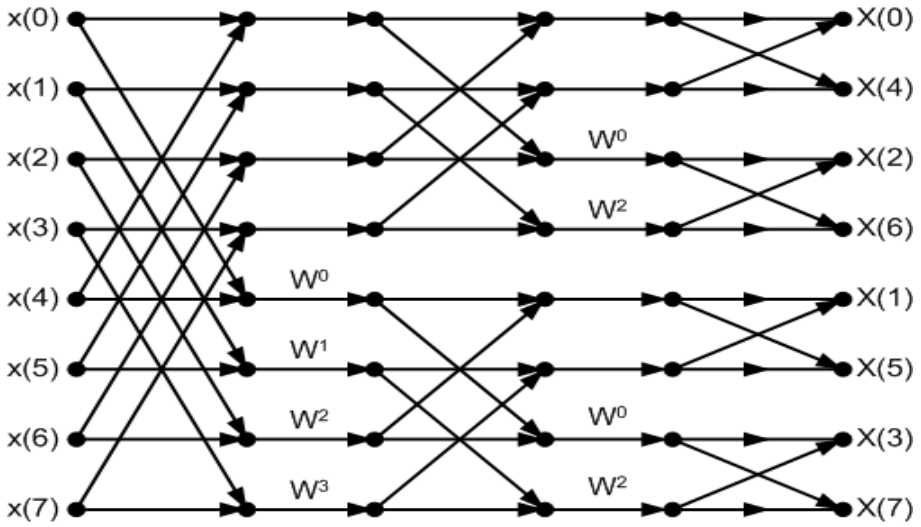

Figure 1: Radix-2 DIF-FFT structure for 8-point

$$X[2k] = \sum_{n=0}^{\frac{N}{2}-1} \left(x(n) + \left(n + \frac{N}{2} \right) \right) W_N^{2nk}$$

$$= \sum_{n=0}^{\frac{N}{2}-1} \left(x(n) + \left(n + \frac{N}{2} \right) \right) W_{\frac{N}{2}}^{nk} \quad (1)$$

$$X[2k+1] = \sum_{n=0}^{\frac{N}{2}-1} \left(x(n) - \left(n + \frac{N}{2} \right) \right) W_N^{2nk}$$

$$= \sum_{n=0}^{\frac{N}{2}-1} \left(x(n) - \left(n + \frac{N}{2} \right) \right) W_{\frac{N}{2}}^{nk} \quad (2)$$

Input of Even frequency signal is mentioned in eqn(1). Similarly the odd input frequency signal is mentioned in eqn(2). Based on the mathematical representation, it only the entire FFT processor is designed. First the initial verification is done theoretically and then the simulation can start.

4. Radix-2 Single Path Delay Feedback Structure

Radix-2 Single-path Delay Feedback FFT is a technique for parallel to estimating the frequency response of discrete timing response. This structure also referred as “stream-like” processing of block-based algorithm. One of the key advantages of R2SDF FFT is processing the data in a parallel manner whenever input points are available. Butterfly structure for R2SDF FFT is illustrated in Figure 2.

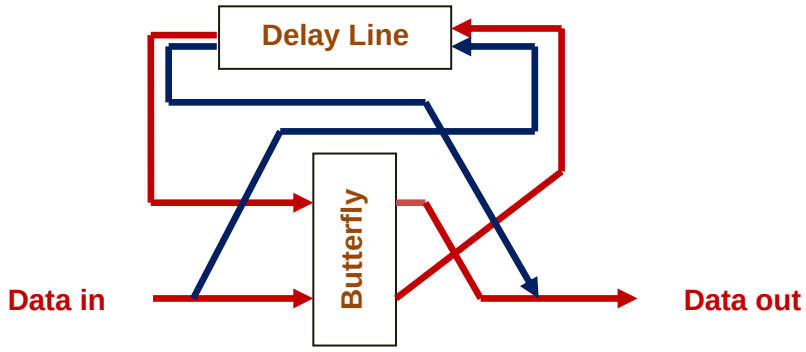

Figure 2: Butterfly structure for R2SDF FFT

It consists of single butterfly structure for performing signed addition and signed subtraction process and a single delay line unit for processing the second point of data, after a single unit delay. In Figure 2 two ways of representations are illustrated to analyze the signal flow of R2SDF FFT.

5. Pipelined Processing Element (PE) Structures for R2SDF FFT

The block diagram of 64-point R2SDF FFT is illustrated in Figure 3. It consists of six processing elements to perform the FFT computation. The input data sequences are divided into two parallel data streams. Six delay units such as 32, 16, 8, 4, 2 and 1 are used to process the two half of the input data sequences at every stage. It composed of three different types of PEs, a complex constant multiplier and delay-line (DL) buffers. Three processing elements PE1, PE2 and PE3 have different architectures to perform the different type of butterfly operations. Among those PE3 structure is used to implement a simple radix-2 butterfly construction and it supplies as the associate modules of the PE2 and PE1 structures.

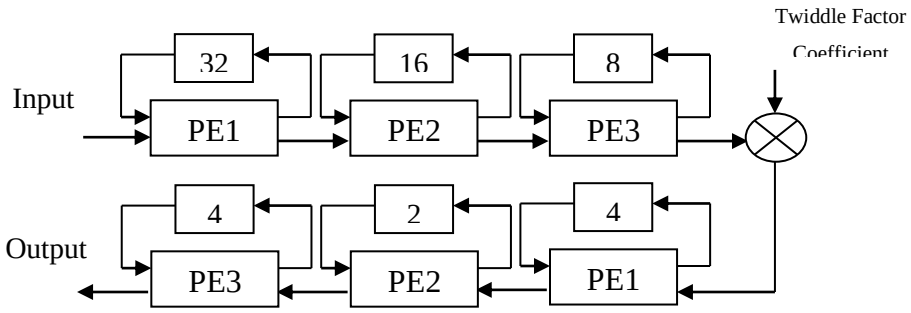

Figure3. Radix-2 Single-path Delay Feedback FFT with Modified BPM

In traditional complex multiplier design, thee multipliers and five adders are used to twiddle factor multiplication of 64-point FFT. In our proposed work, low density adders are identified to reduce the density and hardware complexity of complex multiplication. Hence, this multiplier named as "Reduced Complex Multiplier". In traditional complex multiplier, we identified $i_1 + q_1$ and $i_1 - q_1$ have low density than other adder structures. Hence, in reduced complex multiplier, $i_1 + q_1$ and $i_1 - q_1$ have to be considered as LUT and other elements remain unchanged. Proposed Reduced Complex Multiplier consists of only 3 number of adder and 3 number of multipliers for performing 64-point FFT computation. Hence, reduced complex multiplier consumes less hardware and delay than traditional complex multiplier.

6. Simulation Results and Analysis

Simulation results of proposed modified BPM with Radix-2 SDF DIF-FFT architecture shown in Figure 4. It clearly shows the input and output of the FFT processor. Here using the pipelined FFT for achieving the high speed, each clock cycle has one input; the input contains both the real and imaginary digits. If we are using 8-point FFT the inputs are given to eight clock cycles sequentially. Likewise, the output is generated in the next clock cycle sequentially. This input and output procedure is same for 16, 32, 64 and so on point FFT process.

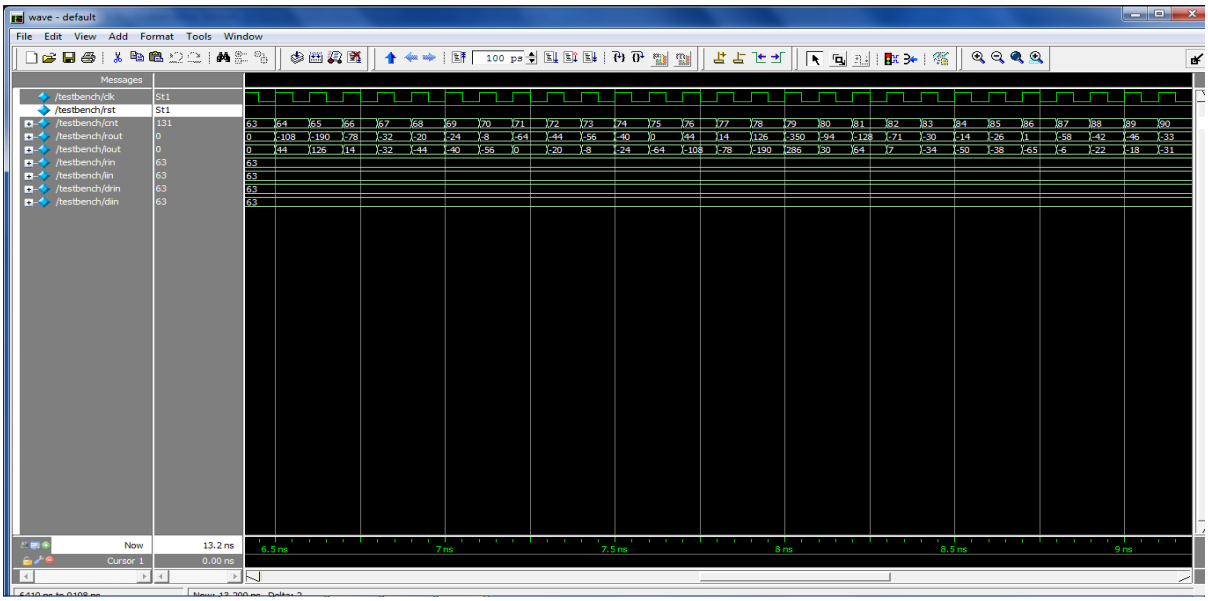

Figure 4: Simulation result of proposed Radix-2 16-point SDF DIF- FFT

Table 1: Comparison Results of R2SDF with ordinary multiplier and R2SDF with Modified BPM

Type	Slices	LUT	Delay (ns)	Frequency (MHz)	Power (mW)
R2SDF FFT with ordinary multiplier	490	864	21.710	46.045	615
R2SDF FFT With Modified BPM	350	590	24.269	41.183	513

Using the Xilinx 12.4 ISE simulator with the Family: Virtex 6, Device: Xc3vlx25tff484-1, Package: PQ208, Speed: -1, the synthesis and implementation results were computed. In Table 1, the performance assessment of Radix-2 SDF with Modified BPM FFT has been compared.

7. Conclusion

In this paper, Radix-2 Single Path Delay Feedback architecture with proposed Modified Bit Parallel multiplier designed using Verilog HDL language. Fast Fourier Transformation (FFT) technique is one of the important frequency transformation techniques in which twiddle factor multiplication performs the conversion process. Twiddle factor is also referred to as rotational factor. In twiddle factor multiplication, the frequency response of corresponding timing signal should be found with the help of amplitude and phase shift of the corresponding signal. Generally SDF architecture is designed for high speed applications. It offers less delay during the computation of FFT process. But one of the main drawbacks is it does not consider the area and power consumption of the FFT. To overcome this fault introduced a bit parallel multiplier for speed up the process and reduced LUT, slices. The SDF structure with Modified BPM offers efficient performance analysis. The designed FFT processor is applied into many applications like MIMO-OFDM, SDR etc. Also the performance is higher when compared with SDF structure with ordinary multiplier.

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