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Tanner Design for Reversible Multiplier

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Abstract: In recent times, power consumption is one of the major drawbacks in both analog and digital circuits. Today all integrated circuits are merged with millions of CMOS transistors. Interconnection of CMOS transistor will drop the power, so to avoid the power without any losses of information. It can design using Mentor graphic tool, one of the famous tool is Tanner EDA mentor graphics. It is clearly showing the power drop at each and every node of the CMOS circuit. Here designs a multiplier for analyzing the multiplier performance. In all digital circuits, the multiplier is a crucial circuit. Tanner EDA mentor graphics provide a new method to build and analyses analogue multipliers. Integrated circuits are made up of millions of transistors and have a large number of wire connections. Multiplier is designed using reversible logic circuit, because it takes less power than the other gates.

Keywords: CMOS, Reversible logic, Tanner EDA, Multiplier, ALU.

1. Introduction

Multiplier is one of the important circuits in all digital circuits. A new way the analog multiplier can be designed and analyzed by using Tanner EDA mentor graphics [1]. Integrated circuits consist of million numbers of transistors, and it has huge number of wire connections [2]. The switching of signal from one node to other node contains some amount of power dissipation, the integrated circuits have lot of signals or information transferred from one node to other node [3]. So, the circuit takes more power, the individual node (CMOS) power is analyzed by T-spice simulation [4]. Here the multiplier is designed using reversible multiplier. It is one of the logics used to recover the output from the input itself [5]. A reverse circuit/gate may create a unique output matrix from each input vector and vice versa, implying that the incoming and outgoing vectors have a one-to-one correlation. As a result, the number of outputs in a reversible gate or circuit is the same as the number of inputs and the only reversible gate is the frequently used classic NOT gate. Each reversible gate has a cost known as the quantum cost [6]. The input values of a bidirectional gate are equal to the number of 2*2 reversible gates or quantum digital logic required in design. One of the most essential characteristics of a reversible gate is its trash output, but it's every input of the gate that is not used as an input to another gate or as a signal source. Many types of logic gates are used to construct the multiplier circuit. The main approach

for reversible logic is it reduces the heat of the device during the internal transformation of information. Heat reduction in the circuit terminates the power dissipation in the device. Reversible logic generates many garbage outputs, some of the garbage outputs are ignored, and it is not considered by the further operations [7].

2. Related Works

The reversible logic based ALU design. The output of the ALU is same as the conventional ALU design. One of the main differences between the conventional ALU and Reversible ALU is internal logic gates [8]. Low power gates are used in the reversible ALU design. HNG, PG, Fredkin and Feynman gates are the most commonly used reversible logic gates [9]. Evaluated the power estimation of CMOS circuit. CMOS transistors are widely used transistor to design the analog circuits [10]. But method has less transition delay and less powers. CMOS schematic is designed by using S-Edit, and the simulation results taken from T-spice. The output waveform is taken from W-Edit [11].

3. Proposed Reversible Logic Multiplier

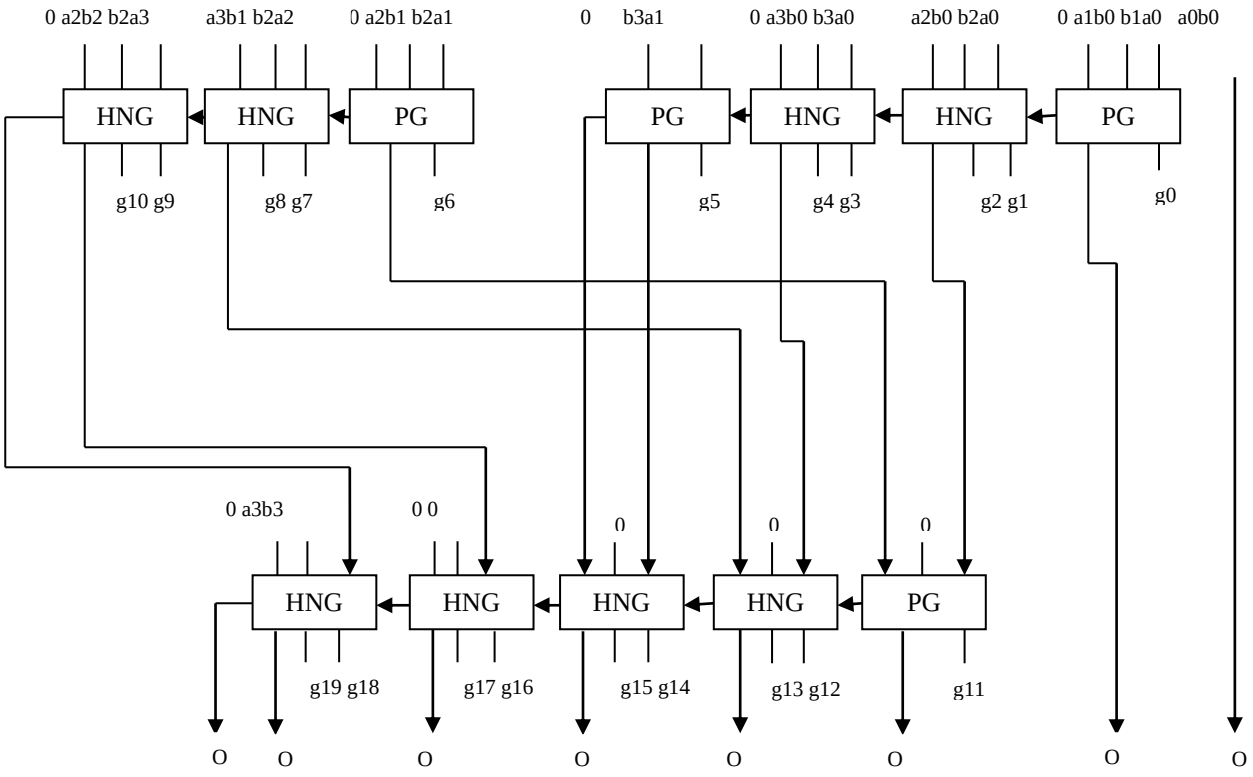

Figure 1.4- Bit Reversible Multiplier

A simple 4-bit multiplier was designed using HNG and PG gate (Figure 1). It is using the four-bit multiplier to enhance the bit to processing the multiplication [12]. In general, the conventional logic gate multiplier uses universal gate [13]. The main aim of the reversible logic is to construct the low power logic circuit. HNG gate is act as a full adder and half adder sum function [14]. So within a single logic function can perform two kinds of operations. The multiplication operation is similar to the irreversible multiplier, but only difference is logic gates [15]. Using the 4-bit multiplier construct the 16, 32 bit and so on multipliers.

4. Results and Discussion

There is now a lot of research going on in the subject of digital circuits, which has low heat dissipation and power efficiency, which is the major reason to use convertible in digital VLSI electronic circuit. The unique gate is used to create efficient partial product modules with the least amount of trash output and gate count. The Inventive0 gate is capable of building a 4-bit ripple carry adder and carry skip that Inventive0 gate is more efficient and optimised thing in terms of gate count, garbage outcomes, and consistent inputs as compared to their previous design.

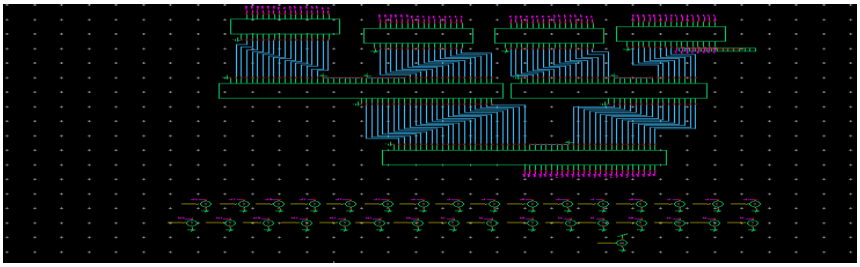

Figure 2. Schematic design of 4-bit Multiplier

The above Figure 2 shows the simulation of schematic design of four-bit reversible multiplier.

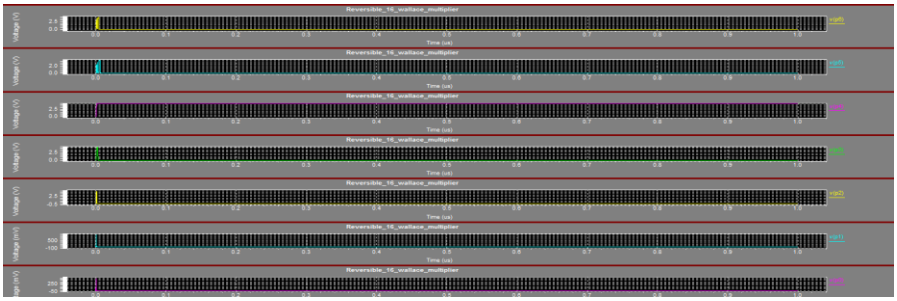

Figure 3. Simulated Output16-bit Multiplier

Table1: Comparison of Reversible multiplier with Normal Multiplier

Parameters	**Reversible Multiplier**	**Irreversible Multiplier**
Look up Tables	34	39
Occupied Slices	18	23
Delay (ns)	6.11	6.24
Power (W)	0.24	0.45

Reversible multiplier reduces the power up to 46.6% and the latency is not that much reduced in the reversible multiplier in Table 1 (Figure 3). Some commonly accessible reversible gates are implemented in the MOS transistor architecture with the goal of minimizing the number of MOS transistors while providing more precise forward and backward calculation. Less structural complexity demonstrates that the revolutionary designs are small, quick, and lower power consumption

5. Conclusion

In this paper, four-bit reversible multiplier was designed for low power application. The power decrease at each node of the CMOS circuit is readily seen. Create a multiplier to assess the multiplier's performance. The multiplier is an important circuit in all digital circuits. Integrated circuits are made up of millions of transistors and thousands of wire connections. There is some power dissipation when switching a signal from one node to another, and integrated circuits have a lot of signals or information to move from one node to another. Tanner EDA mentor graphics offer a novel approach to designing and analyzing analogue multipliers. Integrated circuits feature a great number of wire connections and are made up of millions of transistors. Reversible logic circuits are used to create multipliers because they utilize less power than conventional gates. The comparison table shows the percentage reduction of power for reversible and irreversible multiplier. The performance was analyzed by T-spice tool. The result clearly tells the advantages of reversible logic gate.

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