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DESIGN AND IMPLEMENTATION OF EFFICIENT REVERSIBLE MULTIPLIER USING TANNER EDA

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Abstract - Finite impulse response (FIR) filter is one of the important components in any DSP and communication systems. The output from the DSP processor is depends on the FIR filter, so need an efficient FIR filter design, to achieve an efficient output. Filter architecture contains many components; one of the main components is multiplier. Different types of multipliers are available in the digital circuits, but need an efficient multiplier design to get efficient filters. Multiplier is one of the basic building blocks in the digital circuits. So the performance of the multiplier is important to get an efficient circuit design. Power consumption is one of the major drawbacks in the multiplier. Power consumed by the multiplier is higher in the digital circuits. To overcome the power consumption problem by design an efficient low power multiplier. The low power multiplier is designed by using reversible logic gates. Generally reversible logic was designed by avoiding the higher power consumption by the circuits, compared to Irreversible logic gates, reversible logic consumes less power. To apply the logic in the entire multiplier circuit and see the performance of the multiplier. The low power multipliers overcome the power dissipation in the circuits. It was implemented by using Tanner EDA tool.

Keywords - Reversible logic, Multiplier, FIR Filter

1. Introduction

In VLSI system the Area and power-delay product become the most important parameter of performance. The power dissipation reduction and latency reduction require optimization at all levels of the design procedure. Most of the digital circuit is designed of simple and complex logic gates. Study the best solution to implement multiplier to achieve low power dissipation and high speed. Reversible logic allows designers to implement the subsystem circuits design with zero power dissipation than the existing architecture design. The synthesis of reversible circuit is not easy with the increasing level of device integration and the growth in complexity of circuits, power dissipation, delay and area are the primary goals of design. The failure of high-power circuits relates to the increasing popularity of portable electronic devices. Laptop, pagers, portable video players and cellular phones all use batteries as a power source, in nature battery provide a limited time of operation before they require recharging. To extend life of battery, low power operation is implemented in the integrated circuits. Some application requires more operating power, placing greater demands on energy storage elements in the system. Limitations

of Power dissipation come in two methods. The first method is related to cooling considerations of system when implementing high performance systems. High speed circuits dissipate large amount of energy in a short amount of time, generating a great deal of heat as a by-product.

A gate is reversible if there is a distinct output assignment for each distinct input. Thus, a reversible gate's inputs are uniquely determined from its outputs. A reversible logic gate contains same number of inputs and outputs. Reversible gates are generating the balanced outputs. In a circuit the constant variable is used to balance the output of the circuit. A reversible logic gate contains n number of inputs and n number of outputs with n to n mapping, its helps to determining the inputs and outputs. Extra outputs are added to make the output count equal to the input counts. The main challenges of the gates are memory usage, latency, number of gates and quantum cost.

2. Related Works

Zhijin Guan et al. [1] presented a concept of design the Arithmetic Logic Unit (ALU) based on reversible logic gates. Traditional logic gates were replaced by reversible logic gate, a reversible ALU function is the same as the traditional ALU. The proposed reversible logic decreases the losses of information and the power dissipation of the circuit. Bruce J W et al., [2] proposed the concept of design and implementation of efficient adder circuits based on the HNG gates. HNG and PG gates are proposed to design the low power full adder circuit and have lower hardware complexity.

Power Estimation in Binary CMOS Circuits Based on Multiple-Valued Logic have been presented by Bangyuan et al. [3] this paper presented the use of quaternary and ternary descriptions of signal behavior for power estimation of binary CMOS circuits. A multiple-valued-logic simulation algorithm that can be used at the circuit level, where the MOS device is replaced by a simply modeled device, as well as at the gate level.

3. Irreversible Multiplier

Multiplication is one of the important arithmetic operations in many applications. One of the application are signal processing, communication etc. Signal processing involves multiplication operation, latency and accuracy is the main constraint in the multiplication operation. Array multiplication is performed by using Wallace tree multiplier Wallace multiplication is also knows as parallel multiplier. Array multiplier occupies more number of gates to perform multiplication operation. It occupies large area for computation. This type of multiplier consumes more power when compared to reversible multiplier.

4. Reversible Logic

Reversible logic gate is a successful design to construct a computer for avoids the heat generation problem. Reversible logic is also to improvement in energy efficiency and lifetime of the circuit. Generally energy efficiency is to affect the speed of circuits such as nano electronic and the speed of most computing applications. To increase the portability and scalability of the devices, reversible logic computing is required. The circuit element sizes to reduce the atomic size of the device and the devices become more portable.

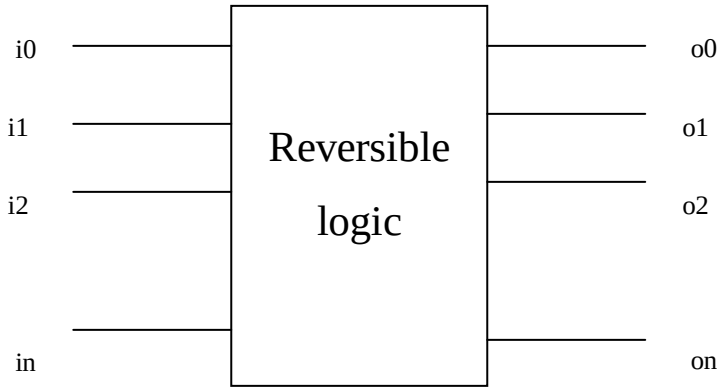

Figure. 1 Reversible Logic gate

The above figure shows the basic function of reversible logic gate. Number of inputs is equal to the number of outputs. Most of the garbage output is ignored from the operations. Different types of logic gates are in the reversible logic named as HNG, toffoli, peres, fredkin, TSG etc. these are the basic reversible logic gate used in the operation.

5. Reversible Multiplier

A four bit multiplier is designed by using reversible logic gates. To replace the functions of normal logic function such as AND, OR, NOT and XOR gate.

These types of gates replaced by reversible logic function. The operation is more or less same as irreversible logic functions. It also provides the same constant output. The design of multiplier using reversible logic gates is done in two parts: partial products generation and operand addition.

In fig.3 shows the circuit diagram of the 4-bit multiplier design using reversible logic gates. Mostly HNG, PG are used to design the multiplier. Different types of logic gates available in the market. Each logic gates have different functions and different characters. Based on the logic

gates only the entire operation is performed. It is mainly used for reduce the power wastage in the digital circuit.

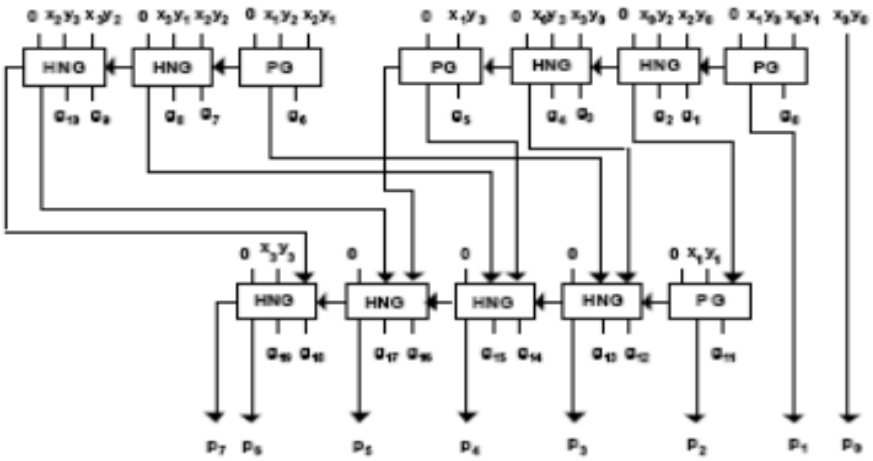

Figure. 2 4-Bit Multiplier using Reversible Logic

6. Simulation Output

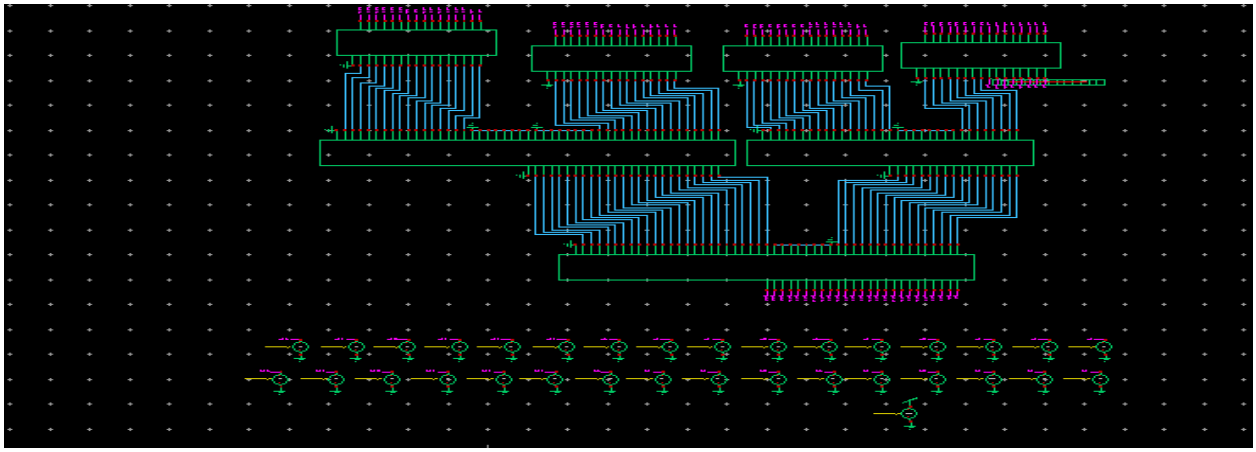

Figure. 3 Design of 4-bit Multiplier

The above figure shows the tanner design of 4-bit multiplier. It uses DC voltage for giving the input to the multiplier.

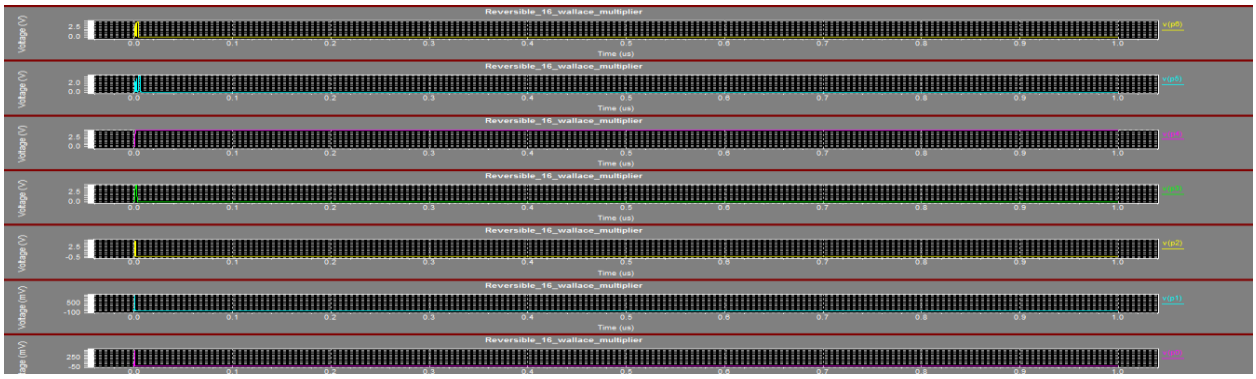

Figure. 4 Simulation Output of 4-bit Multiplier

7. Performance Evaluation

Table No. 1 Comparison between Reversible and Irreversible Multiplier

Parameters	Multiplier using Reversible logic	Multiplier using Reversible logic
Total number of MOSFETs used	19584	19968
Time(seconds)	88.98s	98.22s
Power(watts)	1.96629e-002w	2.052538e-002w

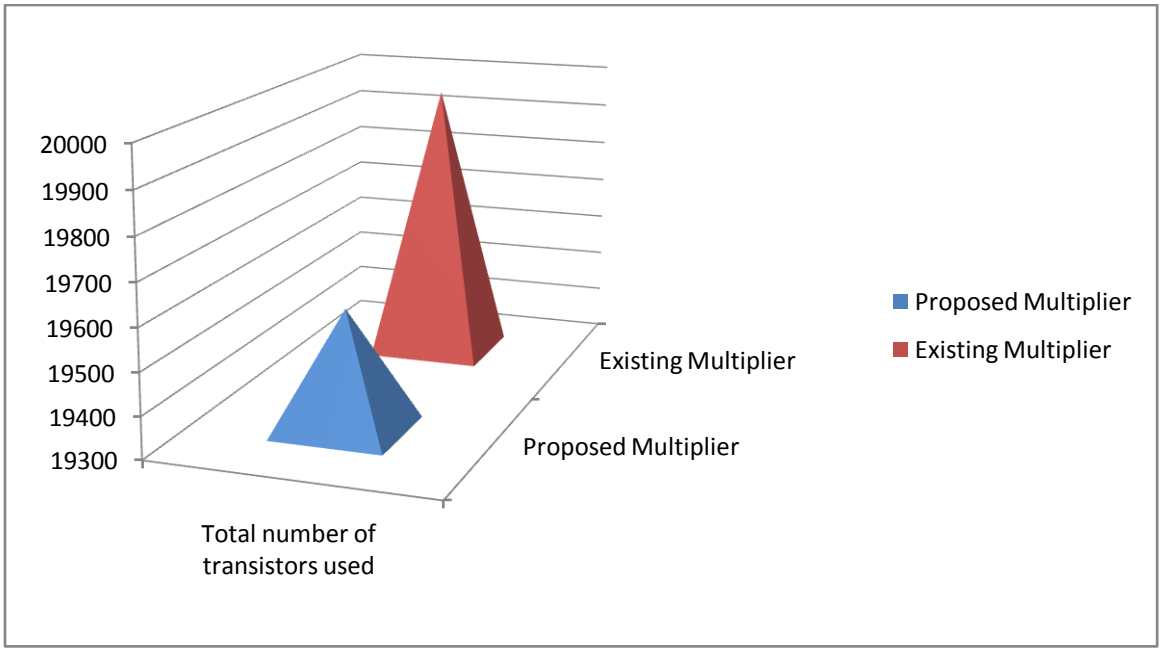

Figure. 5 Area Usages of Both Multipliers

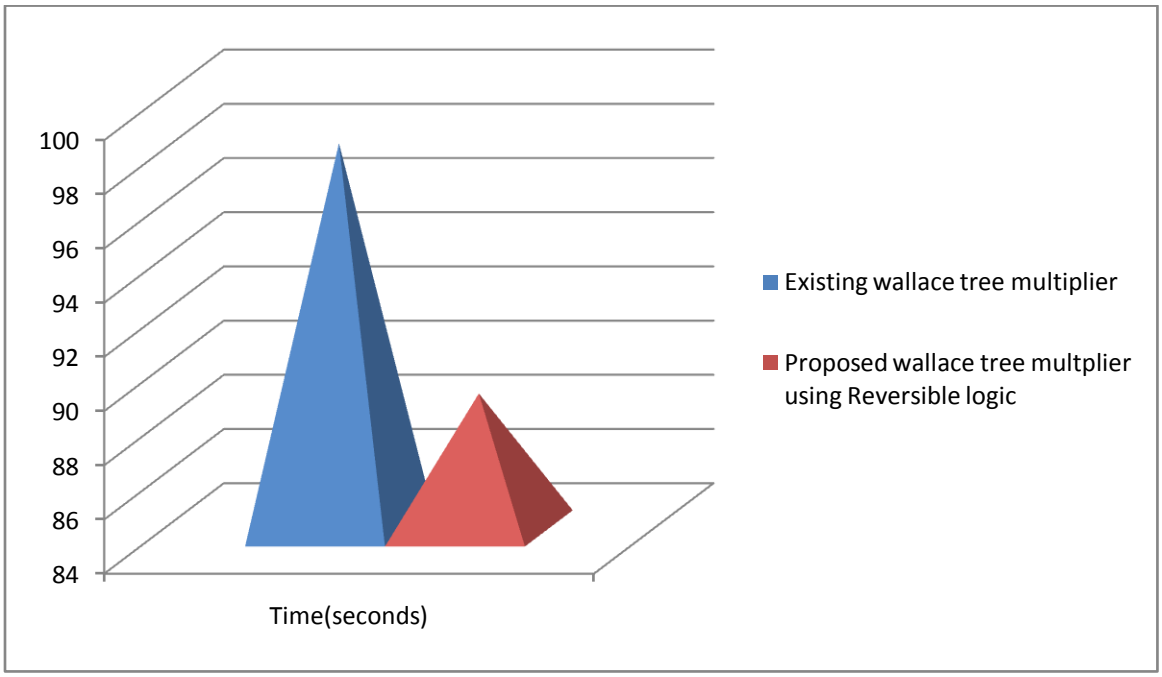

Figure. 6 Delay difference between the multipliers

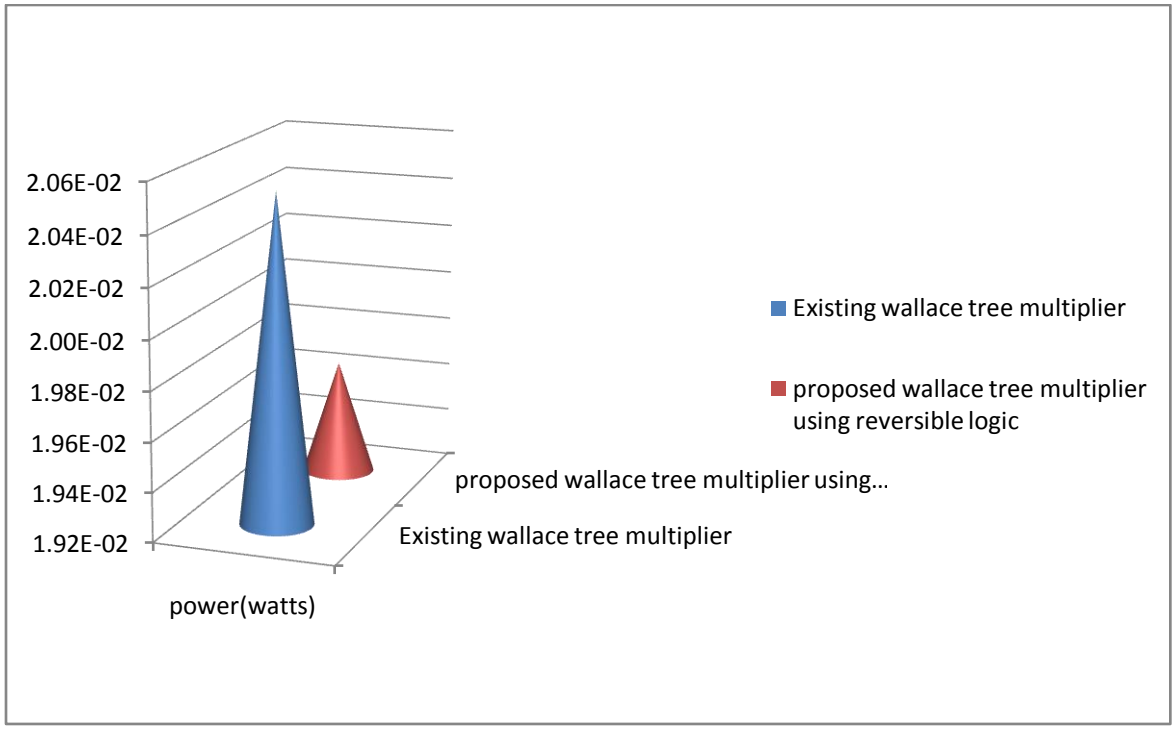

Figure. 7 Power Analyses

8. Conclusion

This paper presents the design and implementation of 4- bit multiplier using reversible and irreversible logic functions. In the reversible logic functions data loss is negligible, when compared to the irreversible logic function, and also the heat generation is zero in the reversible logic function. So the reversible logic gates are used to reduce the power dissipation and consumption in the analog and digital circuits. The proposed reversible multiplier design has low number of garbage outputs and small number of constant inputs. Quantum cost and the number of gates also reduced in the logic function. So the designed proposed logic is used for much application to reduce the power dissipation during the operation.

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