AN ADVANCED SYNCHRONOUS REFERENCE FRAME CONTROL ON REDUCED SWITCH UNIFIED POWER QUALITY CONDITIONER FOR HARMONICS REDUCTION FOR DISTRIBUTION LOAD

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Abstract - This paper is presented a reduced switch count - parallel and series converter is presented in Unified Power Quality Conditioner (UPQC) system. The topology of UPQC is designed with Four-switch in three phase three wire system with series and parallel injection converter connected back to back converter through DC-Link capacitor. Reduced switch count is introduced on both parallel and series converter i.e three phase series and parallel injection converter designed under three phase circuit having 4 switches for two legs of converter and third leg is replaced by capacitor elements. Reduced switch count topology is introduced in the reason for minimizing cost, maintenance, harmonics problems and so improving efficiency of system. The nature of switch replacement by capacitor is an important task to balancing of three phase of each phase voltages. So an ANFIS based synchronous reference frame controller is introduced to balancing of both reduced switch converter and also used to maintained power quality and harmonics minimization. Present controller of ANFIS is combined application of Fuzzy logic and neural network controller so this is used to extract harmonics, disturbances and controlled accurately.

Keywords: Unified Power Quality Conditioner (UPQC), reduced switch three phase back to back converter, ANFIS, power quality, harmonics reduction

1. Introduction

Unified power quality conditioner study explained which UPQC is an ultimate method to improve power quality over power quality disturbances, power factor and harmonics [1]-[4]. UPQC is a combined application and process of STATCOM and DVR. The unified power quality conditioner is prominent solution on power quality issues even at so many FACTS devices are presents in existing nature [5]. Series side converter act as DVR where as parallel side converter act as STATCOM and both are connected as back-to-back converter via DC-Link capacitor [5].

A common application of UPQC are current harmonics minimization across load, real, reactive power control by absorption and injection principles, sag, swell compensation and displacement of unity power factor control [6].DC-Link voltage and its control is a main part of power balances and quality control so this is needed to control at peak value of voltage (phase to neutral voltage) in during power quality disturbances, sag and swell compensation [7]-[9]. So many literatures are explained and provided solution for power quality during unbalances and distorted utility power supply condition [10]-[14]. Injection of Parallel transformer is required for parallel side converter power transformer to inject with high power transmission networks but transformer design in UPQC causes bulky, cost effective and also involved in harmonics because of high frequency components which is constitute the problems concern impregnation of power. Transformer less unified power quality conditioner is presented to overcome above demerits and harmonics reduction by control law and digital mechanism in literatures [15], [16]. A Synchronous Reference Frame (SRF) controller is naturally used to extracting harmonics and distorted content in accurate form from input signals. So based on nature so many conventional methods are described in literatures [17]-[19]. But characteristics and performance of SRF controller is depends on phase lock loop design and its performances so SRF required a suitable phase lock loop system.

The improvement of Unified Power Quality Conditioner (UPQC) is taken to account in latter so reduced switch count is introduces in back to back converter system. The aim of reduced switch count is to reducing switching losses, cost and maintenance reduction and medium power application. This approach is facing a complexity in power flow between series end to parallel end to distribution line. So this paper is proposing a new split phase capacitor introduces as DC-Link for switching action, voltage control and reducing losses. The one of main factor in presented back to back converter is operation and power flow can be control easily while compared with other reduced switch count scheme[21], [22].

This paper is presented a transformer less four wire unified power quality conditioner system for power quality improvement. This paper analyses about harmonics and power factor correction in power quality issues and during distorted and unbalanced supply condition. This topology of improvement is obtained by adaptive network based fuzzy inference system with synchronous reference controller to extract and control of harmonics, power factor correction. Space vector pulse width modulation is applied to both active filters of series and parallel side converter using ANFIS-SRF controller. The proposed controller is used to maintain constant DC-link voltage during disturbances. Space vector scheme is applicable to decoupling of series and parallel converter process with utility line and also this is capable of replacing transformer in present unified power quality conditioner system. Simulation results are obtained and proved using MATLAB/Simulink environment. Design of active and passive filter on UPQC is explained in details in chapter II. The working principle of proposed controller and structures details is given in chapter III. The stepwise performance of topology, parameters details is presented in chapter IV during unbalancing and distributed power supply condition.

2. Design of passive and active series and parallel converter

The filter design aspects enable a little change to the rotating frame as well as the controller design. Y connected LCL filters and delta connected LCL filters design schemes are applied for series and parallel respectively shown in fig. 1. The 5.6KW UPQC is presented with 800V

voltage (line to line, 50Hz). The parameters are listed in the Appendix. The fundamental components of output current for both converter (SSC and S_PC) derived in low frequency. Capacitor branch has been neglected while determine control parameters because it has low pass and high frequency components.

A). The equivalent circuit for LCL Shown in fig. 1 and the filters are inserted between UPQC rotor and S_PC as well as SSC and grid. U_0 Is terminal voltage, U_s is grid voltage, L_1, L_2 and are the converter and grid side inductors respectively. R_3, R_2 are the equivalent resistance between input voltage U_0 and output current I_0 is

$$\frac{R_3 + C_3 s + 1}{L_1 + L_2 + C_3 s^3 (L_1 + L_2) R_3 C_3 s^2 + (L_1 + L_2)s} \tag{1}$$

Equation (1) is a third order transfer function which is offer high attention in high order harmonics with high frequency operation. The inductance value should limit the current ripples of I_1 in the range of 15%-25% of rated current [20]. The current I_1 is mainly depends on impedance X_{L1} (impedance of L_1), X_{L2C3} (impedance of L_2 and C_3) and

X_{c3}(impedance of C_3). Ripple current is derived by PWM frequency is given by

$$\dot{i}_{rip\_max} = \frac{U_{DC}}{8 f PWM\, L_1} \tag{2}$$

Where U_{DC} dc-link voltage and f_{PWM} is converter switching frequency. Based on desired current ripple i_{rip} obtained by

$$L_1 \geq \frac{U_{DC}}{8 i_{ripp} f_{PWM}} \tag{3}$$

In order to avoid voltage drop inductor L is limited and it's given by [18].

$$L_1 \leq \frac{\sqrt{U_{DC}^2 / 3 - U_m^2}}{w_B I_m} \tag{4}$$

U_m Is a peak grid voltage, I_m is a peak grid current and w_B is an angular frequency of grid voltage. High range of capacitor C_3 denotes a low impedance of X_{C3}. C_3 is designed by following

$$C_3 \leq 5\% \times \frac{P_{rated}}{2} \tag{5}$$

$$3 \times 2\pi f B \, U_{rated}$$

Where P_{rated} rated power of converter is, f_B is grid frequency and U_{rated} is RMS value of converter phase**B).**The current ripple reduction (σ) is minimizing through reducing the rate of L_2, C_2 are reduces the current ripple in grid at low level.

$$\sigma = \frac{i_g\left(f_{PWM}\right)}{i_c\left(f_{PWM}\right)} = \frac{1}{\left|L_2 C_3 w_{PWM}^2 - 1\right|} = 10\%$$

(6)

Where $i_g(f_{PWM})$ and $i_c(f_{PWM})$ are the grid current ripple and converter current ripple in the switching frequency limit.

C). Resonance frequency w_{res} fixed between the range of ten times of switching frequency and half of the times of switching frequency are given by

$$10 w_B < w_{res} < 1/2 \, w_{PWM}$$

(7)

Resonance frequency w_{res} for Y connected LCL filters is obtained

$$\sqrt{\frac{L_1 + L_2}{L_1 L_2 C_3}}$$

by

$$w_{res} =$$

(8)

Resonance frequency w_{res} for Δ connected LCL filters is obtained by

$$w_{res} = \sqrt{\frac{L_1 + L_2}{3 L_1 L_2 C_3}}$$

(9)

D). the damping resistor is implemented to reduce the complexity and improve the reliability

of system. Without damping resistor (R_3) in equation (1) becomes

$$R_3 = \frac{1}{3 w_{res} C_s}$$

(10)

One of rapid voltages $\boldsymbol{V_{id}}$ is consist of mean value and oscillation components is given by

$$V_{id} = \tilde{V}_d + \bar{V}_{id}$$

(14)

The reference voltages on load side ($V_{La1b1c1}$)are calculated is given by

$$[V'_{Lb1}] = Trans^{-} \begin{matrix} V'_{La1} & 0 \\ [V_{d}] & \\ V'_{Lc1} & 0 \end{matrix} \quad (15)$$

Inverse transform calculation is described on (16) is applying by mean components across

supply voltage and ωt in proposed ANFIS based SRF algorithm. Direct axis of positive sequence components voltages is calculated by low pass filters which is presented on controller circuit is shown in Fig.2. In equation (13), E_Zro sequence components and negative sequence components becomes E_Zro for control and overcoming an unbalancing, distorted and harmonics on system. A sinusoidal pulse width modulation is generated by

comparing generated reference signals $V'_{La1,Lb1,Lc1}$ with load voltage $V_{La1,Lb1,Lc1}$. The entire controller performance of series side converter is verified across point of common coupling (PCC).

Similarly parallel side converter controller is designed by transform and inverse transform

equation is described bellow in details. Direct I_{id} and quadrature I_{iq} axis current is calculated by comparing oscillation elements I_{id}, I_{iq} and mean elements I_{id}, I_{iq} is given by

$$[I_{id}] = Trans \begin{matrix} I_{i0} & I_{ia} \\ [I_{ib}] & \\ I_{iq} & I_{ic} \end{matrix} \quad (16)$$

The ANFIS based synchronous reference frame controller for parallel side converter current elements of positive sequence is on direct axis elements, negative sequence components is placed on E_Zro and quadrature axis elements for compensating unbalancing and harmonics condition in accurate manner. Active power control is usually obtained by DC-Link capacitor control, so reference voltage V'_{DC} is compared with actual DC-Link Voltage V'_{DC}. Here controlled DC-link current (I_{dloss}) is obtained using ANFIS control topology. Base current components is calculated by summation of active current and controlled DC-Link Current is given as

$$I'_{id} = I_{dloss} + I_{id} \quad (17)$$

Presented series converter control of E_Zro and negative sequence components are set to E_Zro as 0 and quadrature axis elements for compensating harmonics, unbalances and distorted supply utility supply condition.

$$[I'_{ib}] = Trans^{-} \begin{matrix} I'_{ia} & 0 \\ [I'_{id}] & \\ I'_{ic} & 0 \end{matrix} \quad (18)$$

The calculated reference current of utility supply $I'_{ia1,b1,c1}$ is compared with $I_{ia1,b1,c1}$ for generating pulse width modulation for performing series converter operatioS_N and injection to compensating harmonics, real power and reactive power control, distorted and unbalancing utility power supply condition.

2.1 Principles of synchronous reference frame

The presented a modified circuit structure of synchronous reference frame controller is designed by adequate design of phase lock loop design which is shown in Fig.3 (a). Phase lock loop design is designed using adaptive network fuzzy inference system is shown in Fig.3 (b). This ANFIS topology is extracting an accurate reference angle from distorted power supply signals and it's implemented in easy procedure on phase lock loop circuit. reach desired magnitude, and angle by sum function of $\omega 0 = 2\pi f$ calculation of $\omega' t$ is obtained by integrating of function but subtracts lead 90. phase difference to base frequency phasesystem. So angle 90° is needed to subtract from calculated ωt. The calculated form of lock loop reference signals unmovable form when both low frequency level of applying faulty (distorted and unbalancing) signals and auxiliary form of power is turns to E_Zr0.

The calculated signals ωt is a positive sequence form of line voltage or faulty voltages (like wise $\sin(\omega t)$ is a positive sequence component with base frequency of system also $\cos(\omega t)$ is similar form of frequency with sequence components. The overall synchronous reference frame controller is obtained using proposed ANFIS topology with respect to faulty conditioS_N of measured line current. Unique merit of presented control method is not required maximum of measured current over classical schemes. This reference signals generation is capable of controlling unbalancing and distorted line condition by extracting and eliminating harmonics and improving other power qualities.

This control configuration is suitable for extracting power quality disturbances and control of disturbance by generating a suitable reference signal to pulse width modulation scheme in both series side converter and parallel side converter. The generated reference signals is directly compared with sensed signal which load current or supply current. The performance of proposed controller is adopted with proposed configuration circuit under non-liner load condition.

3. Simulation Result

The eight-switch back to back converter is presented to validate performance of unified power quality conditioner and controller performances in power quality aspects. An implementation of presented configuration is carried out using MATLAB/Simulink software in this paper is shown in Fig.4 using the parameters is shown in Table I. The reference signal is generated in Synchronous Reference Frame (SRF) controller using Phase Lock Loop (PLL) circuit. The phase lock loop circuit is a major role in synchronous reference frame controller in nature so adaptive reference frame control scheme is introduced in Phase Lock Loop (PLL) scheme using Rules Table II. Supply and load power performance is carried out in this paper and its analyses under power quality aspects such as harmonics elimination, power factor correction, real power control and reactive power control is shown in from Fig.5-

Table 2. Parameters

	Parameters		Value
Source	Voltage/Power	V_{iabc}	537/5.3kW
	Frequency	f	$50Hz$
Load	Three phase Line Inductance	L_{iabc}	1.47mH
	Three phase load Inductance	L_{Labc}	3.5mH
	DC Line Inductance	L_L	3.5mH
	DC Line Capacitance	C_L	10000uF

DC Link	DC resistance	R_L	500
	Voltage	V_{DC}	210
	capacitance	C_5, C_6, C_{5A}, C_{6A}	1nF
Parallel Side Converter	AC Line Inductance	$L2_{abc}$	3mH
	Filter resistance	$R2_{abc}$	5Ω
	Filter capacitance	$C2_{abc}$	4.7uF
	Switching Frequency	f_{PSC}	20 kHz
Series Side Converter	AC Line Inductance	$L1_{abc}$	1.5mH
	Filter resistance	$R1_{abc}$	5Ω
	Filter capacitance	$C1_{abc}$	26uF
	Switching Frequency	f_{SSC}	12 kHz

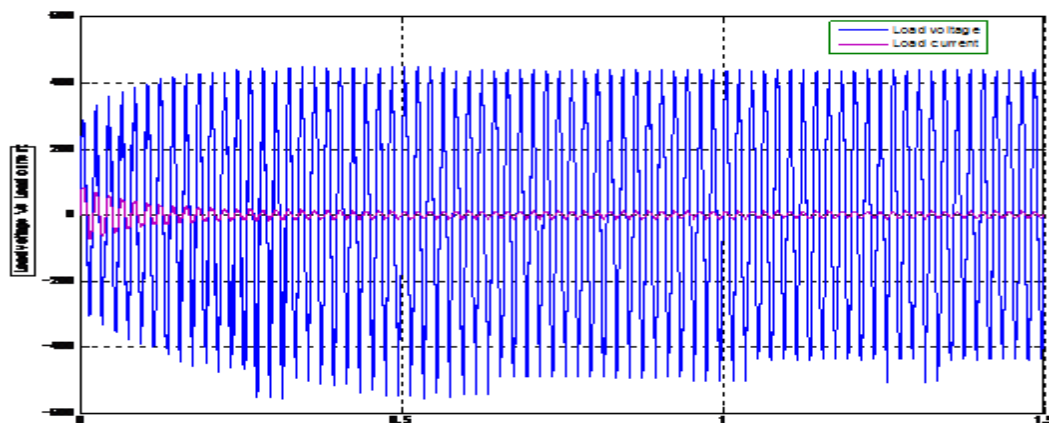Fig.5 power performance: (a) Supply voltage (b) Load voltage (c) supply current (d) Load current
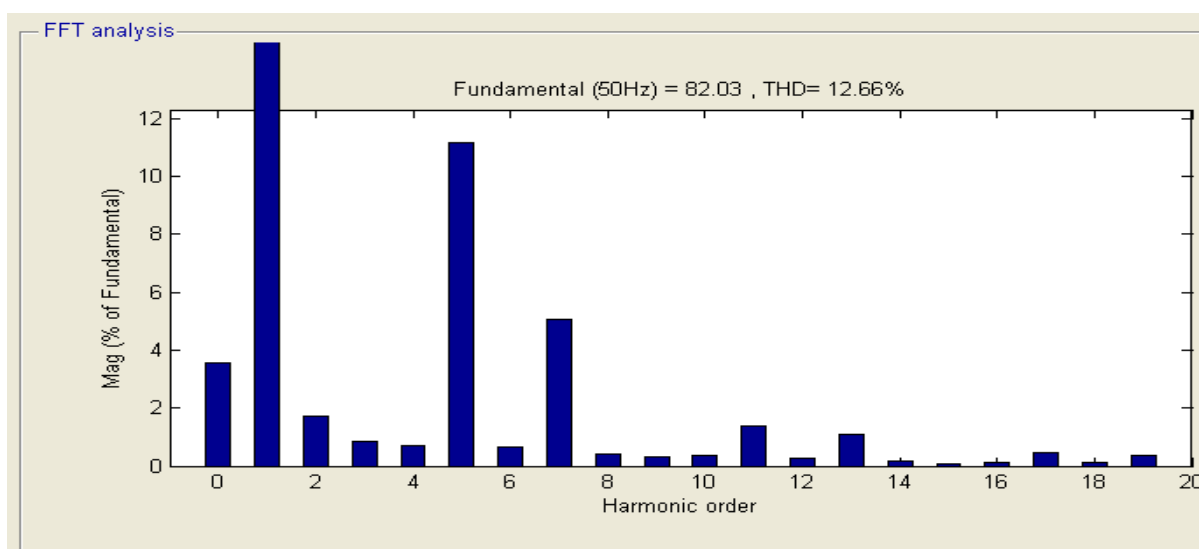

Fig. 6 Power Factor Correction Performance

Fig. 7 Total Harmonics distortion (THD) analysis across load current using FFT analysis

4. Conclusion

The new enhancement of four-switch three phase back to back converter system is introduces in Unified Power Quality Conditioner (UPQC). This topology is offering us a less maintenance, low cost, low power losses and harmonics elimination in medium power application. A common DC-Link split phase capacitor is introduces for both active power control and switching operation of third leg for back to back converter. The control of DC-link capacitor is a challenging task and magnitude control is not been equal over active switching leg so adaptive fuzzy inference based synchronous reference frame controller is presented in this configuration and it is used to improve performance of DC-Link control and converter operation. An investigation of presented topology is carried out using MATLAB/Simulink result and performance is verified in various power quality aspects i.e. harmonics elimination, power balancing and power factor correction.

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