International Journal of MC Square Scientific Research Vol.7, No.1 Nov 2015

FPGA IMPLEMENTATION OF LOW POWER DADDA MULTIPLIERS AND ITS APPLICATION

A. Vincy Beaulah
PG Scholar
Department of ECE
Sree Sastha Institute of Engineering and Technology Chembarambakkam, Chennai.
Email: vincybeaulah@gmail.com

Abstract—Most of the VLSI circuits used adders as a key portion, since they form a base elements of all arithmetic functions. Low power is an imperative requirement for portable multimedia devices employing various signal processing algorithm. We exhibit a new XOR-XNOR component, based on that 4:2 compressor circuit has been designed. The compressor with modified inbuilt logic is proposed for realizations of multipliers. The aim of this paper is to reduce the power consumption of 4:2 compressor without compromising the performance. Power consumption and delay of dadda multiplier using proposed 4:2 compressor have been compared with earlier reported circuits. In digital signal processing application, the FIR filter is designed based on low power proposed approximate dadda multiplier is presented. Simulations are performed using Xilinx ISE 9.2 and microwind tool based on CMOS technology.

Keywords— compressor; Approximate circuit; CMOS; Dadda multiplie; FIR filter.

1. INTRODUCTION

Addition is a fundamental operation in many VLSI systems such as application specific DSP architectures and microprocessors. Multipliers are one of the most important blocks in computer arithmetic used in different digital signal processors. There is growing demands for high speed multipliers in different applications of computing system such as computer graphics, scientific calculation, image processing and so on. Speed of multiplier determines the processors performance and designers are now more focused on high speed with low power consumption. The multiplier architecture consists of a partial product generation, partial product reduction and the final addition. The partial product reduction stage is accountable for a significant portion of the total multiplication delay, power and area. Therefore in order to accumulate partial products, compressors usually implement this stage because they contribute to the reduction of the partial products. Recently, approximate compressors have also gained significance because of their importance in arithmetic operation.

The internal architecture of compressor is fundamentally composed of XOR-XNOR and multiplexer modules. Optimized design of XOR-XNOR module improve the performance of multiplier circuit [2]-[6].In present work, a new XOR-XNOR module has been proposed and approximate 4:2 compressor has been implemented using this module. This proposed circuit

plays an important role in partial product accumulation which reduces transistor count as well as power consumption.

2. COMPRESSOR CIRCUIT BUILDING BLOCKS

The designs of 4:2 compressor circuits are essentially composed of two types of circuits: XOR-XNOR circuits and multiplexer (MUX). Proposed design of XOR-XNOR circuit using eight transistors has been shown in Fig. 1. This circuit provides good driving capability as it uses static CMOS inverter and can operate at low supply voltages. The design has least number of transistors and consumes low power. In this circuit when X1=X2=0 output is low because P1, P2 and N3 transistors are on and logic 0 is passed to output. With input combination of X1=0 and X2=1 circuit show high output as transistor P1, N2 and N3 transistors are on while transistors P2, P3 and N1 are off and high logic is passed to output node. In another case when X1=1 and X2=0, transistor P2, P3 and N1 are on and high logic is passed to output node. In last case when X1=X2=1, output node show low logic as transistor P3, N1 and N2 are on, so proposed circuit works as XOR gate. XNOR operation has been obtained with addition of inverter. Fig. 2 shows the input and output waveforms for XOR-XNOR circuit.

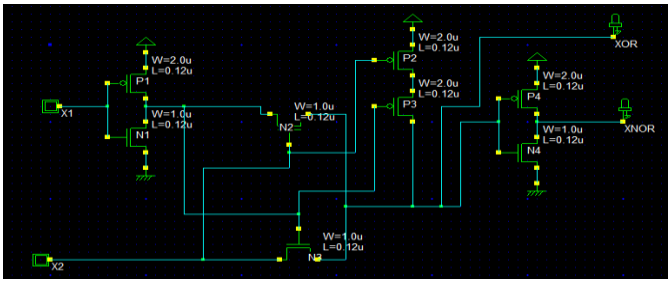

Fig. 1. Implementation of proposed XOR-XNOR circuit

Multiplexer module produces an output that accurately reflects the state of one of the number of data inputs. This accurate output reflection is based on the value of one or more control inputs. The multiplexer generates signals that are produced by carry generator module which is in compressor. Multiplexer with transmission gates shown in Fig. 3 is used in compressor. This design of the multiplexer is faster and consumes less power than the CMOS design [6].

3. EXACT COMPRESSOR

A compressor is a device that diminish n numbers to 2 numbers when properly simulated. A 4:2 compressor plays a prominent role in partial product reduction stage of multiplier. A 4:2 compressor is the broadly utilized structure which has 5 inputs variables X1, X2, X3, X4, C_{in} to generate 3 outputs sum, carry and C_{out} as shown in Fig. 4. The variable C_{in} is the C_{out} generated by previous stage. [7]-[10].

4. PROPOSED APPROXIMATE COMPRESSOR

In the proposed design C_{in} and C_{out} is ignored in the hardware design of approximate 4:2 compressor as shown in Fig. 5.

The architecture of proposed approximate 4:2 compressor has both XOR-XNOR and MUX modules, here the second XOR in the conventional exact compressor architecture is replaced by MUX as shown in Fig. 6 & 7.

A design of an approximate 4:2 compressor increase the performance by reducing the error rate compared with reported circuits. The following expressions describe its output.

The difference between the addition of accurate decimal value of the inputs and the decimal value of the outputs produced by the proposed approximate 4:2 compressor is given as shown in Table II. The design has three incorrect outputs out of sixteen outputs, so the error rate is reduced to 18.75%. The ambiguity of the proposed design is smaller than the other schemes.

TABLE II. TRUTH TABLE OF APPROXIMATE 4:2 COMPRESSOR

Inputs				**Outputs**		
X1	***X2***	***X3***	***X4***	***Sum***	***Carry***	***Difference***
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	0	0	-2

6. SIMULATION RESULTS

The circuits are designed and simulated at 2.25GHz frequency using Microwind tool and the program is synthesized by Xilinx ISE. Comparison of power consumed by XOR-XNOR circuit is shown in Table III. From the table it is clear that proposed XOR-XNOR circuit consumes less power with minimum transistor count.

TABLE III. POWER COMPARISON OF XOR-XNOR CIRCUIT

Design	**Power (µw)**	**Transistor Count**
XOR-XNOR circuit using static CMOS logic	15.440µW	14
XOR-XNOR circuit with 12 transistors	12.593µW	12
Modified XOR-XNOR circuit with 10 transistors	6.593µW	10
Proposed XOR-XNOR circuit with 8 transistors	9.724µW	8

Comparison of power consumed by multiplexer is shown in Table IV. From the table it is clear that proposed multiplexer using transmission gate consumes less power with minimum transistor count.

TABLE IV. POWER COMPARISON OF MULTIPLEXER

Design	Power (µw)	Transistor Count
Multiplexer using standard CMOS logic	11.949 µW	12
Multiplexer using transmission Gates	1.087 µW	6

Comparison of power consumed by 4:2 compressor is shown in Table V. From the table it is clear that proposed approximate 4:2 compressor consumes less power with minimum transistor count. Fig. 15 & 16 shows the input and output waveforms of proposed approximate 4:2 compressor and proposed approximate multiplier. Comparison of dadda multiplier using 4:2 compressor is shown in Table VI. The power delay product comparison of multiplier is shown in Fig. 17.

TABLE V. COMPARISON TABLE OF 4:2 COMPRESSOR

Design	Power (µW)	Delay (ns)	PDP x 10^{-15} (J)	Transistor Count
Exact 4:2 Compressor	23.857	6.743	160.867	42
Proposed Approximate 4:2 Compressor	16.251	6.236	101.341	28

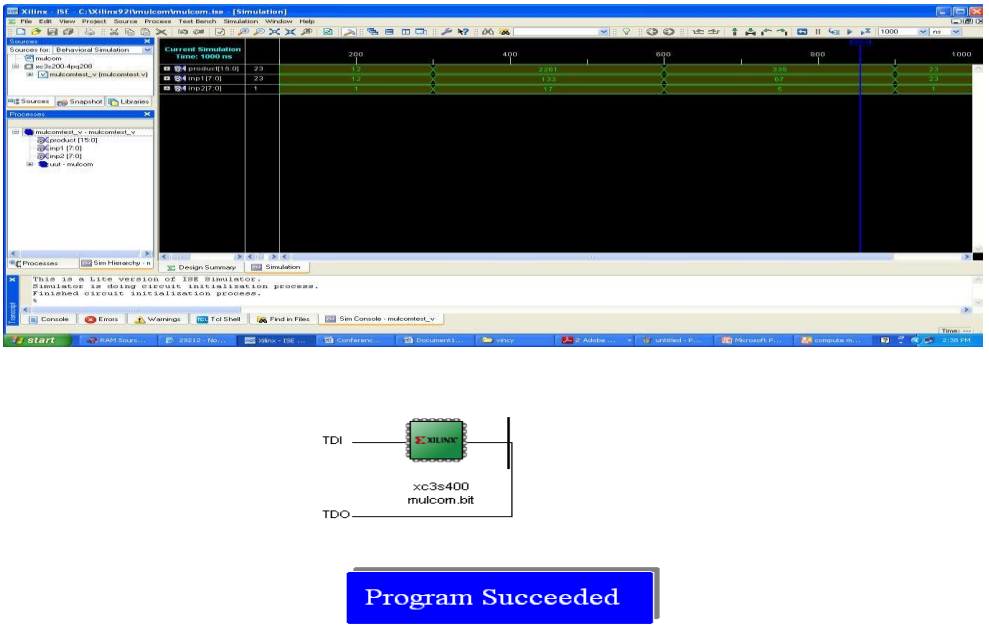

Fig. 16. Input and output waveform of proposed approximate dadda multiplier

TABLE VI. COMPARISON TABLE OF MULTIPLIER

Design	Power (mW)	Delay (ns)
Dadda multiplier using exact compressor	56	30.946
Dadda multiplier using proposed approximate compressor	43	30.374

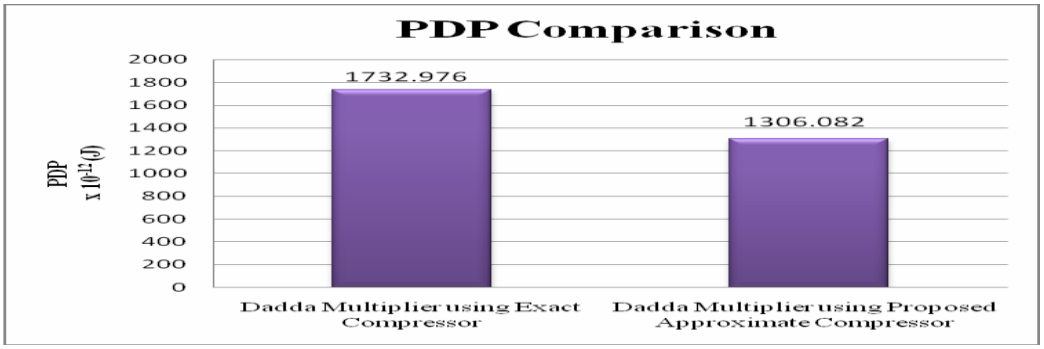

Fig. 17. PDP comparison of dadda multiplier using 4:2 compressor

7. APPLICATION

In this section the application of proposed approximate multiplier in digital signal processing is illustrated. Finite Impulse Response (FIR) filter is one of the primarily used digital filter in Digital Signal Processing (DSP) and communication systems as shown in Fig. 18. The FIR digital filter unit pulse response h(n) is a real numbers, which satisfies both odd and even symmetry.

$$y(n) = \sum_{i=0}^{N-1} h(i)x(n-i) \qquad (6)$$

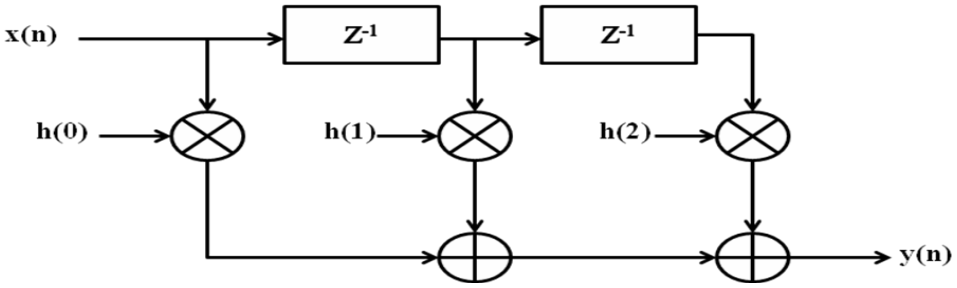

Fig. 18. FIR filter design using proposed approximate multiplier.

The filter is designed using MAC operation, proposed approximate multiplier is used for multiplication. The FIR filter using proposed approximate multiplier run with less processing time. The output waveform of FIR filter using proposed approximate multiplier is shown in Fig. 19.

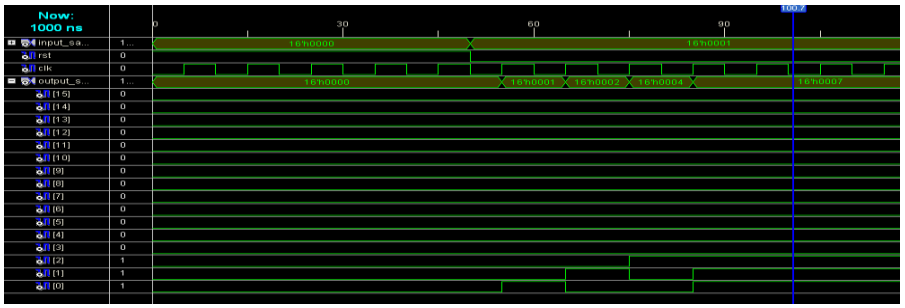

Fig. 19. Output of FIR filter using proposed approximate dadda multiplier.

8. CONCLUSION

An approximate 4:2 compressor circuit based on a new XOR-XNOR design is proposed as it provides better performance. The proposed XOR-XNOR design shows power consumption of 9.724µW with supply voltage of 1.2V. The proposed approximate 4:2 compressor circuit shows power consumption of 16.251 µW with maximum output delay of 6.236 ns. The proposed dadda multiplier uses 6 half-adders, 1 full-adder and 17 compressors. The performance have been compared to earlier reported circuits in terms of power consumption and maximum output delay and implemented in Spartan 3 FPGA. The FIR filter based on proposed approximate dadda multiplier shows better performance than existing in all aspect.

REFERENCES

[1] Wang Z., Jullien G. A., and Miller W. C., "A new design technique for column compression multipliers," IEEE Trans. Comput., vol. 44, pp. 962–970, Aug. 1995.

[2] Weste N., Eshranghian K., Principles of CMOS VLSI Design: A System Perspective, Reading MA: Addison-Wesley, 1993.

[3] Zimmermann R. and Fichtner W., "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid- State Circuits, vol. 32, pp. 1079–1090, July 1997.

[4] Zhang M., Gu J., and Chang C. H., "A novel hybrid pass logic with static CMOS output

drive full-adder cell," in Proc. IEEE Int. Symp. Circuits Syst., pp. 317–320, May 2003.

[5] Manoj Kumar "Design of Novel 9-Transistor Single Bit Full Adder," International Conference on Computational Science, Engineering and Information Technology (CCSEIT-2012), Avinashilingam University, Coimbatore, India. pp. 334-337, Oct. 26-28, 2012.

[6] Shams M., Darwish T. K., and Bayoumi M. A., "Performance analysis of low-power 1-bit CMOS full adder cells,"IEEE Trans. VLSI Syst., vol. 10, pp. 20–29, Jan. 2002.

[7] Hsiao S.F., Jiang M.R., Yeh J.S., "Design of high low power 3-2 counter and 4-2 compressor for fast multipliers", Electronic Letters, Vol. 34, No. 4, pp. 341-343, 1998.

[8] Prasad K., Parhi K.K., "Low power 4-2 and 5-2 compressors", Proceedings of 35th Asilomar Conference on Signals, Systems and Computers, Vol. 1, pp. 129-133, 2001.

[9] Weinberger A., "4:2 Carry-Save Adder Module", IBM Technical Disclosure. Bulletin, Vol.23, January 1981.

[10] Momeni A., Han J., Montuschi P., Lombardi F., "Design and analysis of approximate compressors for multiplication," IEEE Transactions on Computers, in press, 2014.