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Design of an FFT/IFFT Processor for MIMO OFDM Systems

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Abstract

In this paper, we present a novel 128/64 point fast Fourier transform (FFT)/ inverse FFT (IFFT) processor for the applications in a multiple-input multiple- output orthogonal frequency-division multiplexing based IEEE 802.11n wireless local area network baseband processor. The unfolding mixed-radix multipath delay feedback FFT architecture is proposed to efficiently deal with multiple data sequences. The proposed processor not only supports the operation of FFT/IFFT in 128 points and 64 points but can also provide different throughput rates for 1–4 simultaneous data sequences to meet IEEE 802.11n requirements. Furthermore, less hardware complexity is needed in our design compared with traditional four-parallel approach. The proposed FFT/IFFT processor is designed in a 0.13- m single-poly and eight-metal CMOS process. The core area is an FFT/IFFT processor and a test module. At the operation clock rate of 40 MHz, our proposed processor can calculate128-point FFT with four independent data sequences within 3.2 μs meeting IEEE 802.11n standard requirements.

Keywords: 80211n, fast Fourier transform (FFT), multiple-input multiple-output (MIMO) orthogonal frequency-division multiplexing (OFDM).

1. Introduction

The combination of the multiple-input multiple- output (MIMO) signal processing with orthogonal frequency-division multiplexing (OFDM) communication system is considered as a promising solution for enhancing the data rates of the next generation wireless communication systems operating in frequency-selective fading environments. The High Throughput Task Group which establishes IEEE 802.11n standard is going to draw up the next-generation wireless local area network (WLAN) proposal based on the 802.11 a/g which is the current OFDM-based WLAN standards [1]. The IEEE 802.11n standard based on the MIMO OFDM system provides very high data throughput rate from the original data rate 54 Mb/s to the data rate in excess of 600 Mb/s because the technique of the MIMO can increase the data rate by extending an OFDM-

based system. However, the IEEE 802.11n standard also increases the computational and the hardware complexities greatly, compared with the current WLAN standards. It is a challenge to realize the physical layer of the MIMO OFDM system with minimal hardware complexity and power consumption—especially the computational complexity—in VLSI implementation. The FFT/IFFT processor is one of the highest computational complexity modules in the physical layer of the IEEE 802.11n standard. According to IEEE 802.11n standard, the execution time of 128-point and 64-point with 1–4 simultaneous data sequences must be calculated within 3.6 or 4.0 s. Therefore, if employing the traditional approach to solve the simultaneous multiple data sequences, several FFT/IFFT processors are needed in the physical layer of a MIMO OFDM system. Thus, the hardware complexity of the physical layer in a MIMO OFDM system will be very high. This paper proposes an FFT/IFFT processor with a novel multipath pipelined architecture to deal with the issue of the multiple data sequences for MIMO OFDM applications. The 128/64-point FFT/IFFT with 1–4 simultaneous data sequences can be supported in our proposed processor with minimal hardware complexity. Furthermore, the power consumption can also be saved by using higher radix FFT algorithm. The paper is organized as follows. Section II describes the problems of the implementation of the FFT/IFFT processor in a MIMO OFDM system. The 128-point mixed-radix FFT algorithm including radix-2 FFT algorithm and three-step radix-8 FFT algorithm, the 64-point three-step radix-8 FFT algorithm and the IFFT algorithm is described in Section III. Section IV focuses on describing the proposed FFT/IFFT architecture for IEEE 802.11n applications. In Section V, the layout view of the proposed FFT/IFFT processor and the simulation results are presented. Then, conclusions are drawn in Section VI.

2. Design issue of FFT processor for MIMO OFDM system

Jing A block diagram of the receiver of IEEE 802.11n standard is shown in Fig. 1. It contains four RFs, four analog-to-digital converters (ADCs), four FFTs, a MIMO equalizer, four de-qam and de-interleaver, a de-spatial parser, a de-puncturer, a channel decoder, a synchronization block, and a channel estimation block. Depending on the desired data rate, the modulation scheme can be binary phase shift keying (BPSK), quaternary phase shift keying (QPSK), or quadrature amplitude modulation (QAM) with 1–6 bits. The encoding rates in this specification are 1/2, 2/3, 3/4, or 7/8. The number of spatial sequence is supported by 1, 2, 3, or 4. The guard interval period is 400 ns or 800 ns. The bandwidth of the transmitted signal is 20 or 40 MHz The FFT size is 64 points or 128 points. Thus, the FFT/IFFT processor has to calculate 128 points or 64 points with simultaneous 1–4 data sequences within 3.6 or 4 s depending on the number of spatial sequence, the guard interval and the FFT size. In the last three decades, various FFT architectures, such as single-memory architecture, dual-memory architecture [2], pipelined architecture [3], array architecture [4], and cached-memory architecture [5], have been proposed. However, to our knowledge, few papers have reported how to deal with multiple data sequences based on these FFT architectures. In general, multiple FFT processors are added to deal with multiple data sequences in a MIMO OFDM system, as shown in Fig. 1, and therefore cause a

large increase in the hardware complexity and power consumption, compared with that of the single FFT processor. In addition, the throughput rate of the FFT processor for the high-speed WLAN applications is very high. A good FFT processor should not only provide a high throughput rate, but also deal with multiple data sequences effectively for MIMO OFDM applications. In our view, the pipelined architecture should be the best choice for the high throughput rate applications since it can provide high throughput rate with acceptable hardware cost. The pipelined FFT architecture typically falls into one of the two following categories. One is multipath delay commutator (MDC) and the other is single-path delay feedback (SDF) [3]. In general, the MDC scheme can achieve higher throughput rate by using multiple data paths, while the SDF scheme needs less memory and hardware complexity with the delay feedback scheme. Besides, the operation of the complex multiplication consumes lots of power in the FFT processor. In order to save power dissipation, higher radix FFT algorithm can be used to reduce the number of complex multiplications [6]. Three-step radix-8 FFT algorithm is chosen in our design to save complex multiplications. Because 128-point FFT is not a power of 8, the mixed-radix FFT algorithm combining two different FFT algorithms is needed. The mixed-radix multipath delay feedback (MRMDF) FFT architecture can provide higher throughput rate with minimal hardware cost by combining the features of MDC and SDF [7]. However, this scheme cannot deal with multiple input data sequences. The main motivation of this paper is to design a novel unfolding MRMDF structure based FFT processor for MIMO OFDM applications. In our proposed processor, the FFT architecture can not only deal with 1–4 simultaneous data sequences for MIMO OFDM applications but also save lots of hardware complexity, compared with the traditional approach as shown in Fig. 1. Proposed FFT Architecture for a MIMO OFDM System.

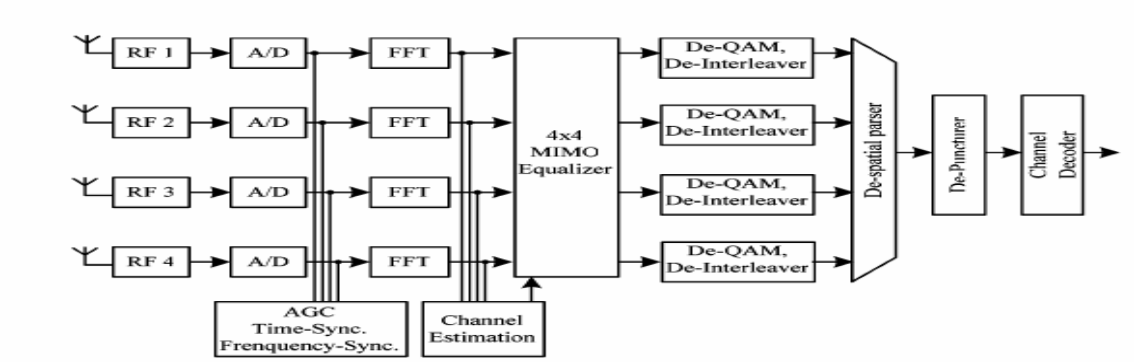

Figure. 1 Proposed FFT Architecture for a MIMO OFDM System

According to (4), (6), and SFG (Fig. 2), we propose a novel 128/64-point FFT/IFFT processor to support 1–4 simultaneous data sequences for a MIMO OFDM system, as shown in Fig. 2. The proposed FFT architecture combining the features of the SDF and MDC architectures

consists of Module 1, Module 2, Module 3, Module 4, conjugate blocks, a division block, and multiplexers. The features of the proposed FFT architecture are as follows.

First, 128-and 64-point FFT with 1–4 simultaneous data sequences can be operated in our design. Second, the proposed FFT architecture can provide several throughput rates to achieve the requirements of IEEE 802.11n standard. Third, the minimal memory is needed by using the delay feedback scheme to reorder the input data and the intermediate results of each module; the hardware complexity of the complex multipliers can be reduced by using the scheduling approach and the specified constant multipliers; so the proposed FFT processor has less hardware complexity, compared with the approach using multi FFT processors. And last, higher radix FFT algorithm can be implemented to save power dissipation regardless of the operation of 64-point or 128-point FFT.

The order of the input sequences and output sequences has the specified order in the proposed FFT architecture. In Fig. 2, the letters, A, B, C, D, mean the different input sequences. The index means the number of FFT points. The index is from 0 to 127 and 0 to 63 for 128-and 64-point FFT, respectively.

Because the order of input sequences, shown in Fig. 2 is the same as that of the data sequences from the ADC, shown in Fig. 1, no extra memory is required to reorder these input sequences before they are loaded into the FFT processor. In general, the order of the output sequences is different from that of the input sequences in the pipelined FFT architecture.

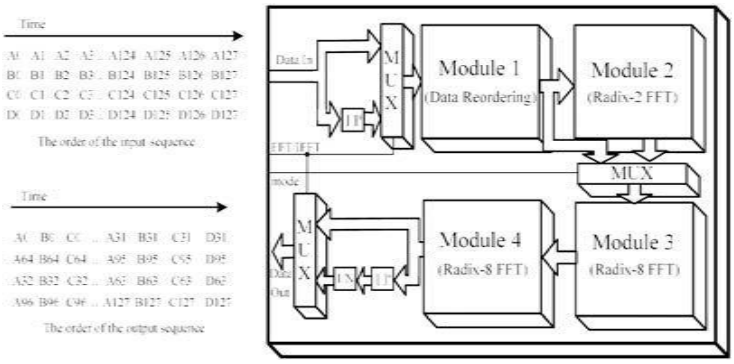

Figure. 2 Block diagram of the proposed 128/64-pointFFT/IFFT processor.

The input order of data in a sequence

	a[6]	a[5]	a[4]	a[3]	a[2]	a[1]	a[0]
Data path	$a[0]_{II}$	$a[1]_{II}$					
1st	0	0	a[2]	a[3]	a[4]	a[5]	a[6]
2nd	0	1	a[2]	a[3]	a[4]	a[5]	a[6]
3rd	1	0	a[2]	a[3]	a[4]	a[5]	a[6]
4th	1	1	a[2]	a[3]	a[4]	a[5]	a[6]

The output order of data in a sequence

Figure. 3 Relation between the input order and the output order of data in a sequence.

And the order of the output sequences is usually dependent on the FFT algorithm, the number of data path, and the FFT architecture. In our design, the order among these four output sequences is the repetition of the order A, B, C, and D, as shown in Fig. 2. And the relationship of the input and output order of data in each data sequence is shown in Fig. 3. The bit-reversal addressing concept is described in detail in [9]. The operation of FFT or IFFT is controlled by the control signal, FFT/IFFT, as shown in Fig. 2. When an IFFT is performed in our processor, the complex conjugate of the input data is taken and they will be performed by the process in treating FFT. Then, the complex conjugate of the output data from FFT will be taken again, and will be divided by 128 or 64 depending on the operation of 128-or 64-point FFT. Because both 128 and 64 are power of 2, the operation of the division is implemented by shifting the decimal point location. The operation of 128-or 64-point FFT/IFFT is controlled by the control signal, mode. If the operation of 64-point FFT/IFFT is performed, the calculated data from Module 1 will skip Module 2 and go into Module 3 directly. The function of Module 1 is to reorder the data among these four data paths into a specific order to implement the operation of FFT/IFFT with multiple data sequences more efficiently. Module 2 is to implement a radix-2 FFT algorithm, corresponding to the first stage of SFG, as shown in Fig. 2. Module 3 and Module 4 are to realize three-step radix-8 FFT algorithm, corresponding to the second and third stages of the SFG, as displayed in Fig. 2. Two different schemes are adopted in Module 3 and Module 4 to implement three-step radix-8 FFT algorithm to minimize the memory requirement and to ensure the correction of the FFT output data.

3. Performance Analysis

In IEEE 802.11n standard, the 128-point and 64-point FFT/IFFT are used for the bandwidth of 40 and 20 MHz, respectively. And 1–4 simultaneous data sequences must be supported in this specification according to the number of antennas used. Eight operation modes of the FFT/ IFFT processor are needed in IEEE 802.11n standard, as listed in Table I. Two operation clock rates of our scheme, 40 and 20 MHz, are needed for the operation of 128-point and 64-point FFT/IFFT. The effective throughput rates of our design are de pendent on the number of data sequences and can be calculated as

$$\text{Effective throughput rate} = 4R \times \text{operation ratio} \quad (7)$$

where the operation ratio is defined as the number of data sequences divided by 4. In general, while the number of data sequences is less than four, the number of operations is less than four in each group. So the effective throughput rate will be less than number of data sequences is three, only three operations are needed in each group. So the operation ratio is 3/4 and the effective throughput rate is equivalent.

Operation mode		Operation clock rate (R)	Effective throughput
No. of FFT point	No. of input sequence		
128	4	40 MHz	4R
128	3	40 MHz	3R
128	2	40 MHz	2R
128	1	40 MHz	1R
64	4	20 MHz	4R
64	3	20 MHz	3R
64	2	20 MHz	2R
64	1	20 MHz	1R

Figure. 4 Performance of operation modes in our proposed FFT architecture

4. Simulation and implementation

At first, the 128/64-point chosen FFT/IFFT algorithm is coded by MATLAB language. After the chosen FFT/IFFT algorithm is valid, the architecture of the processor was modeled in Verilog and functionally verified using Verilog- XL simulator. The word length of our proposed FFT processor is a parameter which can be decided by customers. Based on the simulation results, we determined the word length of the proposed FFT/IFFT to be 12 bits in both real and imaginary parts to meet IEEE 802.11n system requirements. According to the operation clock rate lists in Table I, two clock rates, 40 and 20 MHz, are used for the operation of 128- point and 64-point FFT. And the input sequences are in the specified order when they are loaded into the proposed FFT processor, as shown in Fig. 3. At the operation clock rate of 40 MHz, the computation of 128-point FFT/IFFT with four data sequences requires 3.2 s, i.e., 128 cycles. Furthermore, the computation of 64-point FFT/IFFT with four simultaneously data sequences needs 3.2 s at the operation clock rate of 20 MHz Due to the execution.

5. Conclusion

A novel 64/128-point FFT/IFFT processor for a MIMO OFDM system has been proposed. In our design, 64-point and 128-point FFT/IFFT can be supported. Based on the concept of data reordering and grouping, the processor can provide different throughput rates to deal with 1–4 simultaneous data sequences more efficiently. Furthermore, the hardware costs of memory and complex multiplier can be saved by adopting delay feedback and data scheduling approaches. And the number of complex multiplications can be reduced effectively by using

higher radix FFT algorithm. The proposed FFT/IFFT processor designed in a 0.13- m 1P8M CMOS process can meet IEEE 802.11n standard at the operation clock rate of 40 MHz.

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