International journal of mc square scientific research, Vol 1 , June 2009

BIST for system-on-a-chip using an embedded FPGA core

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Abstract

Embedded memories in FPGAs have evolved over each new generation. Several FGPA vendors have sophisticated memories within their devices. Such devices are the Virtex series from Xilinx, the Stratix series from Altera, and the AT40k family of FPGAs from Atmel. These embedded memories are highly programmable and offer the user many options such as selectable word depth and data width. Other modes of operations include built in FIFO support and cascadability with adjacent rams along with several more features.With all of these integrated features, a method for testing this memory resource is required. These algorithms are applicable to testing memory resources in FPGAs. The main concern in testing memory resources is the test time required to detect all faults. Using the latest Virtex 4 FPGA as model, this paper will discuss a BIST methodology for testing memory resources by which a specific set of march tests is used to completely test the memory resource and at the same time minimize the time needed for testing.

1. Introduction and background

Memory resources in FPGAs have become a major component in FPGAs over each new generation. The Virtex 1 FPGA from Xilinx was released in 1998 and the largest version, the XCV1000, contained 131,072 bits of dedicated memory resources or as Xilinx calls them, block RAMs [1]. The newest FPGA from Xilinx, the Virtex 4 (V4) contains almost 76 times that amount. At 9,936Kbits of block RAM (18K each), the Virtex 4 FX140 is quite possible the largest FPGA currently manufactured [2].

2. Overview of March algorithms

In [2], van de Goor describes a march algorithm named March LR. It is described as a complete test for simple faults and realistic linked faults. Van de Goor defines simple faults as the set of faults which include the following: address decoder faults (AF), single cell faults, and

faults between memory cells. Single cell faults can further be classified into subclasses which include the following: stuck-at-faults (SAF), stuck-open faults (SOF), transition faults (TF), and data retention faults (DRF). Likewise, faults between memory cells can further be classified as coupling faults (CF), inversion coupling faults (CFin), idempotent coupling faults (CFid), state coupling faults (CFst), and disturb faults (CFdst). Linked faults are defined as the occurrence of two or more simple faults. Van de Goor also reduces the set of linked faults to what is called a realistic set of linked faults. CFins, two linked CFids, and two linked CFdsts are the faults removed from the linked fault set leaving the remaining linked faults to be called realistic linked faults. The March LR test is given in the above figure. Van de Goor also shows that this test sequence is superior to March C-, which is a popular testing algorithm in industry [4]. March LR can detect certain static NPSFs that March C- is unable to detect [2].

March lr with bds

As In [3], Van de Goor describes a method for efficiently converting a bit-oriented memory march test such as March LR and March C- to word-oriented memory (WOM) tests. WOM march tests can detect inter-word faults (faults among words) and intra-word faults (faults within words). V4 block RAMs have the ability to address words within a line of memory. In a 512 x 36 configuration, there are four words and a parity bit for each word [5].

In order to sensitize intra-word CFs, a variation of the usual all zero or one test pattern is needed. Instead of zeros and ones, Goor describes a sequence of bits that is called a background data sequence (BDS). Table 1 shows a BDS for an 8- bit word. These sequences are similar to a walking 1s /0s approach, but the BDS Goor gives is a more optimal sequence. This sequence can be applied to all words in an address location. Since all words should have the same BDS, a march test designed to detect single bit SAFs will detect any mismatch between words as well [5]. As March LR's complexity is on the order of 14*N, where N is the number of address locations. Converting March LR to a WOM is (51* N / 8) which is given by the formula {(16 + 7 * log2(B))* n / B}, where B is the bit length of the word and N is the number of address locations [5].

MATS+

The MATS+ memory test algorithm is the simplest march test to detect all AFs for memory resource. This march test will be performed directly following the March LR with BDS. All faults within the memory array should be detected after March LR with BDS. MATS+ is needed to exercise the programmable address decoder in each of the remaining configurations (1k x 18 – 16k x 1).

S2PF AND D2PF

In [1], Hamdioui and Van de Goor describe a fault model for two-port memories. In this model they define two types of faults likely to occur in dual-port memories: Strong faults and

weak faults. Strong faults are those faults which can be sensitized by using a single-port (SP) test such as those described previously. Weak faults are defined as a fault partially sensitized during an operation. Only when multiple weak faults are sensitized does a fault become visible. Such multiple weak fault sensitization can occur in dual-port operations. Hamdioui and Goor show that two types of march tests are needed to provide fault coverage in two port memories. March s2PF[7].

Application to virtex 4 blocks rams

The subset of V4 block RAM functionality previously defined contains the functionally for which the March tests have been described. What is needed though is a mechanism by which to apply the discussed march tests. In [8], a circular BIST approach is used for testing embedded cores in SoCs. A similar architecture would be quite sufficient in implementing BIST for V4 block RAMs. In Figure1, a BIST architecture is given. Each half of the V4 has its own Test Pattern Generator (TPG) that drives the block RAMs in its respective half [9]. The output response analyzers (ORAs) compare the output from each block RAM with the output of an adjacent block RAM. The ORAs on the left and right edge are compared with each other which yield the aforementioned circular BIST.

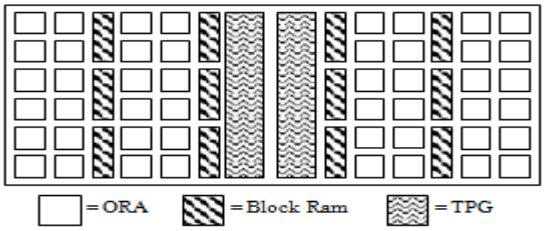

Figure 1 – Memory BIST Architecture

The TPG for this BIST architecture must be able to generate a sequence of different march tests. The mode bit vector allows the user to set the March test to be performed. The addition of dual address and data lines provides support for the needed dual port testing. Also, the TPG must be able to provide control lines on all active levels (active high / low and rising/falling clocks) since V4 block RAMs provide this programmability. Varying active levels should be tested during the many BIST cycles the TPG will generate.

3. Performance analysis

In [8], Stroud and Garimella give a BIST methodology for testing block RAMs in the Virtex 2 series FPGA. As this V2 BIST is similar to the V4 BIST architecture, a comparison of the expected performance should be beneficial.

BIST	Test Algorithm	Address Locations (*A*)	Data Width (*D*)	Clock Cycles
1	March LR w/ BDS	512	36	58×*A*
2	MATS+ [8]	1K	18	5×*A*
3		2K	9	5×*A*
4		4K	4	5×*A*
5		8K	2	5×*A*
6		16K	1	5×*A*
7	March s2pf-	512	36	14×*A*
8	March d2pf	512	36	9×*A*
TOTAL BIST CLOCKS= 200192				

Table 1 – V4 BIST Performance

BIST	Test Algorithm	Address Locations (*A*)	Data Width (*D*)	Clock Cycles
1	March LR w/ BDS	512	36	58×*A*
2	March LR	1K	18	14×*A*
3		2K	9	14×*A*
4		4K	4	14×*A*
5		8K	2	14×*A*
6		16K	1	14×*A*
7	March s2pf-	512	36	14×*A*
8	March d2pf	512	36	9×*A*
TOTAL BIST CLOCKS= 485,888				

Table 2 – V2 BIST Performance

From Tables 1 and 2, it is clear that the selection of MATS+ improves the performance by over 100%. Successive March LR tests do not improve fault coverage as the first March LR with BDS detects all the faults a regular March LR would except for test for AFs in additional configurations. The real performance advantage of the V4 RAM BIST is that the TGP does not have to be changed during the BIST. Partial reconfiguration allow the BIST to only reconfigure the block RAMs to a different configuration and notify the TPG which march test to apply.

4. Conclusion

Several March algorithms in testing literature have been examined and an efficient methodology for testing V4 block rams has been discussed. It should be noted that since the TPG for the BIST is written in VHDL, it is highly portable between FPGA architectures such as those in the Stratix II and AT40K FPGAs. Increasing the efficiency of testing memory resources beyond what is presented and what is has been done previously will be a more difficult process as new FPGA architecture emerge and subsequently become more complicated. However, the most appreciable simplification would be to have empirical data for a certain device that shows the type of faults likely to occur and model march tests at that level.

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