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DESIGN OF AREA EFFICIENT R2MDC FFT USING OPTIMIZED COMPLEX MULTIPLIER

[1] K. Hanumantha Rao, [2] Dr.C.Kumar Charlie Paul
[1]Research scholar, St. Peter's University, Chennai, Tamilnadu, India.
[2]Principal, A.S.L. Pauls College of Engineering and Technology, Coimbatore.

Abstract-Fast Fourier Transformation (FFT) algorithm is the frequency transformation technique in which time domain representation of sampled signal is converted into frequency domain representation of sampled one. In this paper, low complexity Radix-2 Multi-path Delay Commutator (R2MDC) FFT frequency transformation technique is developed through Very Large Scale Integration (VLSI) System design environment. Low power consumption, less area and low delay are the main concerns in VLSI. Traditional Radix-2 MDC FFT structure has more hardware complexity due to its intensive computational elements. In general, complex multiplier structure of R2MDC FFT requires more LUTs and slices than other structure. In order to overcome this problem, complex multiplier architecture of R2MDC FFT is effectively optimized in this paper. Proposed optimized complex multiplier architecture consumes less hardware complexity than existing one. Further, design of R2MDC FFT architecture by using optimized complexity multiplier offer more advantages. Simulation results for proposed low complexity R2MDC FFT architecture is evaluated by using Model-Sim6.3C and synthesis results are evaluated by using Xilinx 10.1 design tool.

Keywords: Fast Fourier Transform (FFT), Complex multiplier, Radix-2 Multi-path Delay Commutator (R2MDC) FFT, low complexity R2MDC FFT, Very Large Scale Integration (VLSI).

1. Introduction

Fast Fourier Transformation (FFT) technique is used to convert the discrete frequency samples into discrete time samples (conversion of frequency to time signals). Normal algorithm for Radix-2 FFT has more computational path to convert the frequency domain signal into time domain signal. In addition, normal algorithm for Radix-2 FFT requires more hardware complexity to implement the design. It is essential that timing based system design to reduce the computational path of FFT algorithm. This section discusses different architectural oriented FFT models to increase the performance in terms of hardware complexity, delay and power consumption. In an arithmetic FFT algorithm, two important processes are used to compute the frequency response of discrete timing responses; these are signed additions/subtractions and twiddle factor multiplications. Divide and Conquer techniques are used to perform the DFT computation. Further, Bit Parallel Multiplication (BPM) has been used to perform twiddle factor multiplication. Based on different butterfly structures, a specific DSP processor have been designed such as general purpose programmable DSP processor, programmable specific FFT processor and algorithm specific processor. In each of the processor, some crucial logics have been used to find the required specified results. In FFT calculation, twiddle factors are used to

find the frequency response of discrete timing points. Fixed twiddle factor values are used for fixed sequence of input points.

2. Related Works

In the brief of Adiono, K, (2012), 64-point FFT design is provided by using Radix-4 algorithm. Most prior endeavours have been developed the best complex multiplier design for Decimation in Frequency (DIF) FFT, i.e. conversion of frequency to time. But this brief gives the complex multiplication design for Decimation in Time (DIT) FFT, i.e. conversion of time to frequency. In addition, Address Generation Unit (AGU) is developed first time in this review. The results for butterfly structures, AGU, control units are simulated and validated by using proper simulation tools.

In the design of Akshata, A, (2012), Radix-4 64 point pipeline FFT/IFFT processor has been developed for 3G and 4G wireless application. One of the key factors of Wireless application is the OFDM System. Similarly, IFFT/FFT is one of the key procedures for OFDM Systems. IFFT is the process of converting frequency spectrum into discrete time oriented signals which is used in transmitter side of OFDM System whereas FFT is the process of converting time oriented signals into frequency spectrum which is used in receive side of OFDM System. In this design, periodicity properties of twiddle factors and reconfigurable complex multiplier are used reduce the ROM size for storing twiddle factor values. The result of this productive modification on FFT architecture reduces the hardware complexity effectively.

In the study of Angeline, T, (2013), realization is made on the structure of butterfly to improve the performance of FFT. The structure of butterfly structure consist of real addition, signed complex multiplication and real subtraction processes. For instance, Radix-4 FFT processors have $3N/4 \log_4 N$ complex multiplications and $3N \log_4 N$ complex additions. In this study, number of complex multipliers and complex adders, Memory size and Control logics are compared for different types of FFT architectures such as R2SDF FFT, Radix-4 SDF (R4SDF) FFT, Radix-4 Single-path Delay Commutator (R4SDC) FFT, Radix-2^2 SDF (R2^2SDF) FFT, Radix-2 Multi-path Delay Commutator (R2MDC) FFT and Radix-4 MDC (R4MDC) FFT.

Adaptive frequency transformation technique is designed with the help of Radix-2 and Radix-4 FFT architecture. From the consideration it is clear that Radix-4 structure have the half of the computational complexity of Radix-2 FFT architecture. But radix-2 FFT architecture has simple dataflow path or processing element architecture whereas Radix-4 architecture has more complexity in processing element unit. Hence, based on these two dependable advantages and disadvantages, an adaptive IFFT/FFT model is designed in this research work. Traditionally Signal to Noise Ratio (SNR) or Bit Error Rate (BER) of the Modulation signal is considered as one of the thresholds in adaptive OFDM technique.

Radix-8 algorithm is used to implement 64-point FFT function. The sequential block has been designed and implemented in the proposed SDF FFT architecture. It requires 6 stages for

implementing 64-point FFT structure. Also different types of feedback structures in Radix-2 such as R2SDF, R2^{2}SDF, R2^{2}SDC is used in the field of wireless communication process. Also new processing elements called R2^{3}SDF, R2^{3}MDC are used to design the memory-based FFT architectures. When compared to Radix-2 processing element, Radix-4 processing element architectures, R2^{2}SDF and R2^{3}SDF FFT architectures provide best VLSI performances in terms of less hardware utilization, low delay & high speed and lower power consumption.

3. Discrete Fourier Transformation

Fourier Transformation process is defined as the conversion process of time domain signal into frequency domain signal and vice versa. The normal N-point DFT is defined as follows,

$$X[k] = \sum_{x=0}^{N-1} x_n W_N^{nk} \quad , \text{k = 0, 1, 2 ... N-1}$$

Where, x_n is defined as the input signals, X[k] is the Fourier transformation of input signal x_n. N is the number of input points. $W_N^{nk} = e^{\frac{j2\pi nk}{N}}$ is the twiddle factor or rotational factor. Twiddle factor is used to determine the frequency response of corresponding discrete time input response. Also it is called as DFT coefficients which have the constant values for N-point FFT. Twiddle factor also described as a "rotating vector" which rotates in increments corresponding to the number of samples.

Function of FFT Coefficients W_N^{nk}

In FFT calculation, twiddle factors are used to find the frequency response of discrete timing points. Fixed twiddle factor values are used for fixed sequence of input points. These factors are also called as "Rotational Factor" which illustrated in figure 1.2. The value for rotational factor lies between '0'and '1'.

For certain values of the product nk, the sine and cosine functions take on the value 1 or 0 (property 1), eliminating the multiplications, as shown below:

$$A \times W_N^{nk} + B \times W_N^{nk+N/2} = \left(A + B \times W_{N/2}^{N/2}\right) \times W_N^{nk} = (A - B) \times W_N^{nk}$$

$$A \times W_N^{nk} + B \times W_N^{nk+N/4} = \left(A + B \times W_N^{4}\right) \times W_N^{nk} = (A - jB) \times W_N^{nk}$$

The computational time of those twiddle factor based multiplication is proportional to N^2. But, periodicity of the complex sequence W_N^{nk} can be achieved significantly by reducing the redundant computational paths.

$$A \times W_N^{nk} + B \times W_N^{n(k+N)} = (A + B) \times W_N^{kn}$$

Where n = 0, 1, 2..... N-1.

Further symmetry property is used to further reduce the complex multiplications. The reduction of complex multiplication by using symmetry property as shown in below:

$$W_N^{nk+N/8} = -W_N^{nk+5N/8} = \frac{\sqrt{2}}{2}(i-j)\times W_N^{nk}$$

$$W_N^{nk+3N/8} = -W_N^{nk+7N/8} = \frac{\sqrt{2}}{2}(i+j)\times W_N^{nk}$$

The twiddle factor multiplication of equation (1.10) consists of two real multiplications and two real additions. Thus, the symmetry utilization of phase difference ± 45° only requires two real multiplications and two real additions. For instance, Signal Flow Graph (SFG) structure of 16-point DIF FFT is shown in figure 1.3. The output of DIF FFT is bit reversal in nature. It represents the frequency representation of timing signals. To perform 8-point FFT calculation, it requires three stages.

4. MDC Structure

In order to reduce the required chip size of FFT computation, more number of delay elements is inserted in MDC FFT. Therefore, more number of independent blocks can be processed in a parallel manner. Due to more number of delay elements, speed of MDC is comparatively low. However, the chip size and power consumption of MDC FFT can be improved significantly. If implemented as presented, the pipeline has 50% hardware utilization. The first butterfly is idle half of the time until it can process new pairs of inputs. All hardware operates at input sample frequency. Situation can be easily improved by duplicating input buffer and operating it in ping-pong fashion. Hardware utilization jumps to 100%.All hardware operates at half the sample frequency. In R2MDC FFT structure, input sequence is broken into two parallel data streams flowing forward with correct “distance” between data elements entering the butterfly scheduled by proper delays. Both multipliers and butterflies are less utilization in R2MDC FFT structures. In abovefig, C2 represents the commutator structure and BF2 represents the butterfly structure.

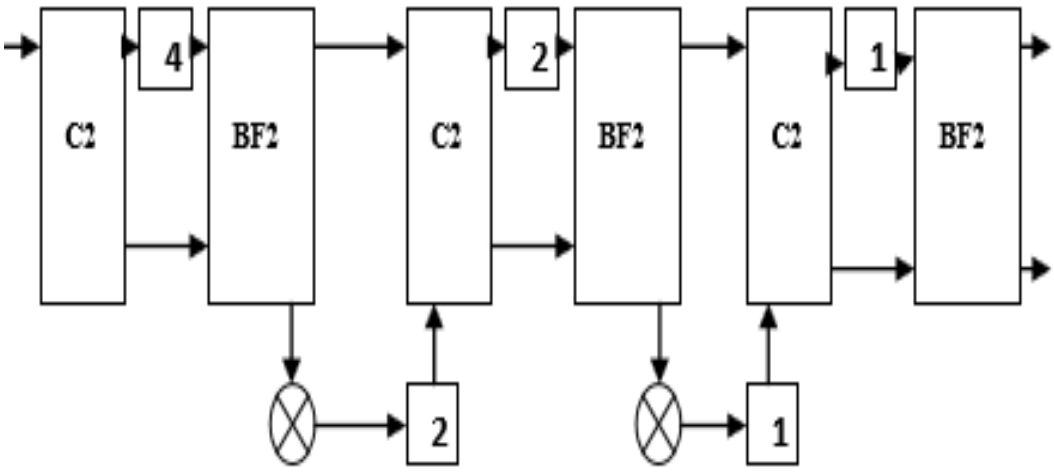

Fig. 1 Structure of MDC

Twiddle factor multiplication is used to compensate the frequency domain and time domain signal, in the place of twiddle factor multiplier use the Modified Bit Parallel Multiplier (MBPM). It has been used for calculating the multiplication results. Two main number of twiddle factor values such as 0.707 and -0.707 are involved in the complex multiplication of FFT structures. Modified BPM structure for the twiddle factor value 0.707 has been illustrated in Figure. When integrating this modified BPM structure into R2SDC FFT structure, the performances has been improved than Mixed R2SDC FFT structure. In addition pipelined registers are used to reduce the delay and improve the speed of the processor further.

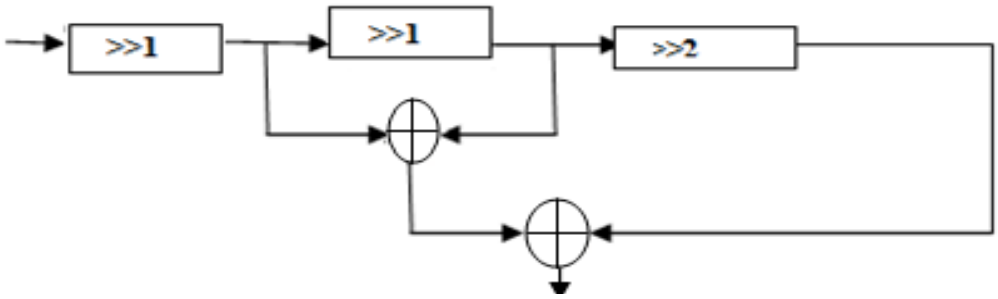

Fig. 2 Modified BPM structure for the twiddle factor value 0.707

5. Simulation Results

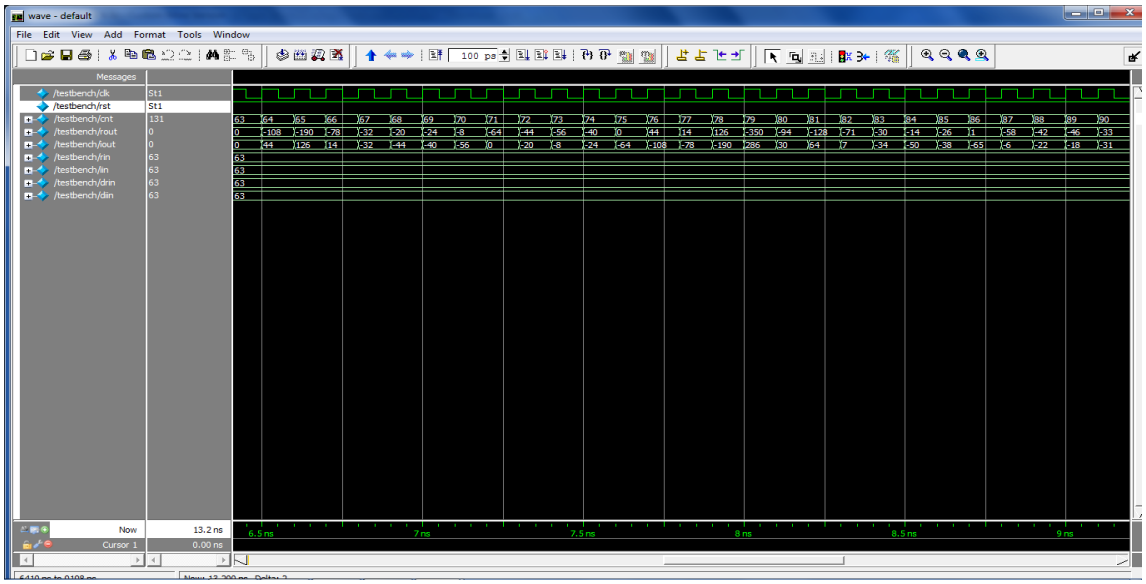

Fig. 3 Simulation Result of R2MDC

5. (A) Performance Analysis

Table.1 Comparison between Existing and Proposed FFT

Parameters	Traditional R2SDC FFT	Proposed R2MDC FFT	Percentage Reduction
Slices	616	576	6.49%
LUTs	1195	1122	6.10%
Delay (ns)	53.341	53.307	Slightly reduced

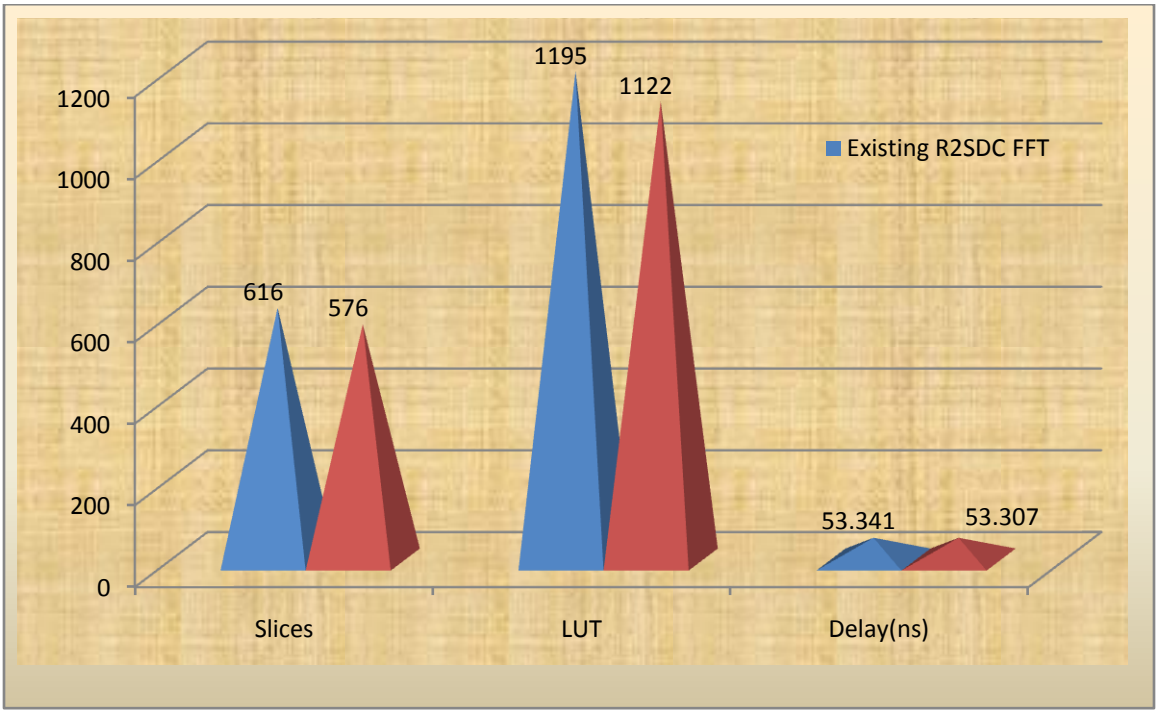

Fig. 4 Graphical Comparison between Existing and Proposed FFT Structure

In figure. 3 show the simulation results of Radix-2 MDC structure. The simulated results are taken from modelsim 6.3c. The results are analyzed by Xilinx 10.1 ISE tool. The analyzed results and differences are clearly shown in the table no.1

6. Conclusion

In this paper, an adaptive FFT technique has been proposed by using R2MDC FFT. Hence, it is used to make an adaptive FFT system. From Xilinx synthesis results, it is clear that R2MDC FFT offers 6.45% improvements in hardware slices, 7.67% improvements in LUTs and slightly improvements in delay than R2SDC FFT. In other hand, R2SDF FFT offers improvements in speed of the operation than R2MDC FFT. From the described results, it is clear that both R2SDF and R2MDC FFT have different types of advantages. Based on these different advantages different types of environment adopt different advantages based frequency transformation techniques. Hence it is essential a less area utilization based frequency transformation technique to transmit the information signal. Based on different requirement, SDF and MDC based dataflow structures are used effectively.

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