



VLSI BASED Mixed-Radix 8-2 Butterfly FFT with bit reversal for 802.11a

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Abstract

OFDM has received a great deal of attention and been adopted in many new generation wideband data communication systems such as IEEE 802.11a. In these communication systems the different applications mentioned above have different demands in operation speed and length of FFT/IFFT. The modified Mixed Radix 8-2 Butterfly FFT with bit reversal for the output sequence derived by index decomposition technique is our proposed VLSI system architecture to design the prototype FFT/IFFT processor for OFDM systems. In this paper the analysis of FFT algorithms such as mixed radix 4-2 and mixed radix 8-2 were designed using VHDL. The results show that the proposed processor architecture can greatly save the area cost while keeping a high-speed processing speed, which may be attractive for many real-time systems. By using the proposed structure, the proposed algorithm makes an offer the simple bit reversal mechanism which is only supported by a fixed radix FFT algorithm.

Key words: OFDM, FFT/IFFT, VLSI, VHDL, Mixed Radix with bit reversal.

1. Introduction

Fast Fourier transform (FFT) are widely used in different areas of applications such as communications, radars, imaging, etc. One of the major concerns for researchers is the enhancement of processing speed. Several methods of for computing FFT (and iFFT) are discussed. These are basic algorithms for implementation of FFT and iFFT blocks. While there has been extensive research on the theoretical efficiency of these algorithms (traditionally algorithms have been compared based on their floating point operation counts), there has been little research to-date comparing algorithms on practical terms. The choice of the best algorithm for a given platform is still not easy because efficiency is intricately related to how an algorithm can be implemented on a given architecture.



In this paper, a mixed radix 8-2 butterfly structure with simple bit reversing for output sequences derived by index decomposition technique is presented. The new method to obtain the mixed radix butterfly structure with simple bit reversing for output sequence is established. Therefore the proposed mixed radix 8-2 offers a engineering insight of general mixed radix.

2. FAST FOURIER TRANSFORM

The Discrete Fourier Transfer (DFT) plays an important role in many applications of digital signal processing including linear filtering, correlation analysis and spectrum analysis etc.

The DFT is defined as:

$$X[k] = \sum_{n=0}^{N-1} X[n] W_N^{nk} \quad k = 0, 1, \dots, N-1 \quad (1)$$

Where

$W_N^{nk} = e^{-j\frac{2\pi}{N}nk}$ is the DFT coefficient.

Evaluating the Equation (1) directly requires N complex multiplications and $(N-1)$ complex additions for each value of the DFT. To compute all N values therefore requires a total of N^2 complex multiplications and $N(N-1)$ complex additions. Since the amount of computation, and thus the computation time, is approximately proportional to N^2 , it will cost a long computation time for large values of N . For this reason, it is very important to reduce the number of multiplications and additions.

3 Mixed Radix 4-2

A mixed radix algorithm is a combination of different radix- r algorithms. That is, different stages in the FFT computation have different radices. For instance, a 64-point long FFT can be computed in two stages using one stage with radix-8 PEs, followed by a stage of radix-2 PEs. This adds a bit of complexity to the algorithm compared to radix- r , but in return it gives more options in choosing the transform length. The Mixed-Radix FFT algorithm is based on sub-transform modules with highly optimized small length FFT which are combined to create large FFT. However, this algorithm does not offer the simple bit reversing for ordering the output sequences.

4 Mixed-Radix 4-2 FFT Algorithms with Bit Reversing

The mixed-radix 4/2 butterfly unit is shown in Figure 1. It uses both the radix-2² and the radix-2 algorithms can perform fast FFT computations and can process FFTs that are not power of four. The mixed-radix 4/2, which calculates four butterfly outputs based on X(0)~X(3). The butterfly unit has three complex multipliers and eight complex adders. Four multiplexers represented by the solid box are used to select either the radix-4 calculation or the radix-2 calculation.

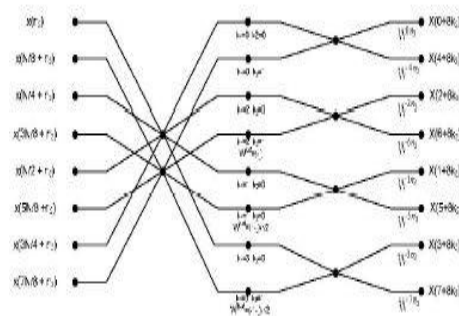


Fig 1: The basic butterfly for mixed-radix 4/2 DIF FFT algorithm.

5 Mixed-Radix 8-2 FFT with Bit Reversing output sequences for 64 points FFT

In order to verify the proposed scheme, 64-points FFT based on the proposed Mixed-Radix 8-2 butterfly with simple bit reversing for ordering the output sequences is exemplified. As shown in the Figure 1, the block diagram for 64-points FFT is composed of total six-teen Mixed-Radix 8-2 Butterflies. In the first stage, the 64 point input sequences are divided by the 8 groups which correspond to $n_3=0, n_3=1, n_3=2, n_3=3, n_3=4, n_3=5, n_3=6, n_3=7$ respectively. Each group is input sequence for each Mixed-Radix 8-2 Butterfly. After the input sequences pass the first Mixed-Radix 8-2 Butterfly stage, the order of output value is expressed with small number below each butterfly output line in the figure 2. The proposed Mixed-Radix 8-2 is composed of one radix-8 butterflies and four radix-2 butterflies. In the first stage, the input data of one radix-8 butterflies which are expressed with the equation $B_4(o, n_3, k_j) B_4(i, n_3, k_1)$, are grouped with the $x(n_3), x(N/4 \pm n_3), x(N/2 \pm n_3), x(3N/4 \pm n_3)$ and $x(N/8 \pm n_3), x(3N/8 \pm n_3), x(5N/8 \pm n_3), x(7N/8 \pm n_3)$ respectively. After the each input group data passes the first radix-8

butterflies, the outputted data is multiplied by the special twiddle factors.. The order of the output sequence is 0,4,2,6,1,5,3 and 7 which are exactly same at the simple binary bit reversing of the pure radix butterfly structure. Consequently, proposed mixed radix 8-2 butterfly with simple bit reversing output sequence include one radix 8 butterflies, four radix 2 butterflies, one multiplier unit and additional shift unit for special twiddle factors. The proposed Mixed Radix 8-2 butterfly unit has two complex multipliers and eight complex adders.

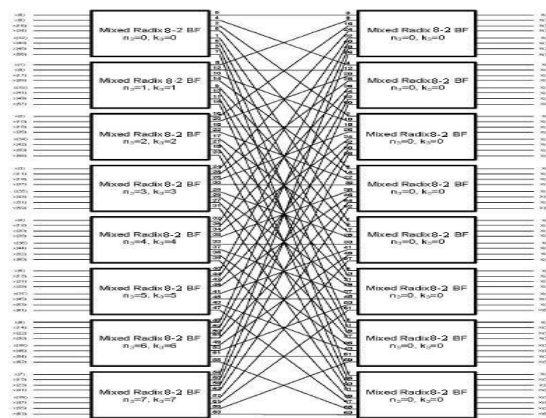


Fig.2 Proposed Mixed-Radix 8-2 Butterfly for 64 point FFT

6 RESULT

Employing the parametric nature of this core, the OFDM block is synthesized on one of Xilinx’s Virtex-II Pro FPGAs with different configurations. The results of logic synthesis for 64 point FFT based orthogonal frequency division multiplexing (OFDM) using Mixed Radix 4-2 and mixed radix 8-2 are presented in Table 1. We analysis the 64-point FFT based ofdm is chosen to compare the number of CLB slices and Flip Flop for different FFT architectures .

64 point FFT	CLB Slices/7680	Utilization factor	Power in mW
Mixed Radix 4-2 FFT	754	9.98%	3832.79mW
Mixed Radix 8-2 FFT	599	7.89%	2697.51mW

Table 1: Comparison of FFT Algorithm based on CLB Slices, DFF, Function Generators



7 Conclusion:

In this paper, The FFT algorithms considered here include mixed-radix 4/2 and mixed radix 8-2 which is the subject of this study. In contrast, mixed radix 8-2 FFT algorithm is capable of producing hardware with structural regularity. It is more efficient than radix-2 FFT algorithm and applicable to all 2^n -point FFT systems. Moreover, the proposed technique makes an offer systematic viewpoint in the Mixed-Radix algorithm. The proposed Mixed Radix 8-2 butterfly unit has only two complex multipliers and eight complex adders. Reduction in area and power can further leads to less implementation cost.

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