# Study and Survey about Mixed Radix FFT Processor in MIMO OFDM

N.Kirubananda Sarathy          Karthikeyan Kottaisamy          M.Rajmohan
Research Scholar,              Scientist ABB                   Asst Prof, ECE
St.Peters University,          Chennai.                        Hindustan University
Chennai.                                                       Chennai

*Abstract*—

The design of a highly configurable continuous flow mixed-radix (CFMR) Fast Fourier Transform (FFT) processor is presented in Multi-Input Multi-Output (MIMO) Orthogonal frequency division multiplexing (OFDM). Multi-Input Multi-Output (MIMO) system has drawn much attention in 4G wireless technologies. Orthogonal frequency division multiplexing (OFDM) is a popular method for high data rate wireless transmission. OFDM may be combined with antenna arrays at the transmitter and receiver to increase the diversity gain and enhance the system capacity on time variant and frequency selective channels, resulting in Multi-Input Multi-Output (MIMO) configuration. This paper represent as  Mixed radix FFT  in MIMO-OFDM system design including channel modeling, space time block code techniques, channel estimation and signal processing algorithms used for performing time and frequency synchronization in MIMO-OFDM system.

## 1. Introduction

Orthogonal frequency division multiplexing (OFDM) and space-time coding have been receiving increased attention due to their potential to provide increased capacity for next generation wireless system. OFDM supports high data rate traffic by dividing the incoming serial data streams into parallel low-rate streams, which are simultaneously transmitted on orthogonal sub-carriers .For large enough and a sufficiently large guard interval, the channels as seen by each of the sub-carriers become approximately frequency flat and allow for high order modulation. Due to this desirable feature, OFDM has been adopted in many commercial system such as the IEEE 802.11a, ETSI HIPERLAN type2 wireless LAN system and DAB, DVB-T broadcasting systems. Space-time coding is a communication technique for wireless systems that

50

realizes spatial diversity by introducing temporal and spatial correlation into the signals transmitted from different transmits antennas. Many space-time trellis and block codes have been proposed for flat fading channels. Most significantly, Alamouti discovered a very simple space-time block codes (STBC) for transmission with two antennas guaranteeing full spatial diversity and full rate. It lends itself to very simple decoding and has been adopted in third generation (3G) cellular systems such as W-CDMA. Recently many literatures proposed Space-time block coding schemes applicable to OFDM systems based on the Alamouti scheme . When channel can be assumed to be approximately constant during to consecutive OFDM symbol durations, the Alamouti scheme is applied across two consecutive OFDM symbols and is referred to as the Alamouti STBC-OFDM or simply A-STBC-OFDM. The combinations of the Multiple- Input Multiple – Output (MIMO) signal processing with orthogonal frequency – division multiplexing (OFDM) communication system is considered as a promising solution for enhancing the data rates of the next generation wireless communication systems operating in frequency-selective fading environment the high Throughput Task Group which establishes IEEE 802.11n standard is going to draw up the next generation wireless local area network (WLAN) proposal based on the 802.11a/g which is the current OFDM-based WLAN standards. The IEEE 802.11n standard based on the MIMO-OFDM system provides very high data throughput rate from the original data rate 54 Mb/s to the rate in excess of 600 Mb/s because the technique of the MIMO can increase the data rate by extending an OFDM-based system. However the IEEE 802.11n standard also increase the computational and hardware complexities greatly, compared with the current WLAN standard. It is a challenge to realize the physical layer of the MIMO-OFDM system with minimal hardware complexity and power consumption. The FFT/IFFT processor is one of the highest computational complexity modules in the physical layer or the IEEE 802.11n standard .If employing the traditional approach to solve the simultaneous multiple data sequences, several FFT processors are needed in the physical layer of a MIMO OFDM system. Thus the hardware complexity of the physical layer in MIMO OFDM system will be very high. This paper proposes as FFT processor with novel multipath pipelined architecture to deal with the issue of the multiple data sequences for MIMO OFDM applications. The 128/64 FFT with 1-

51

4 simultaneous data sequences can be supported in our proposed processor with minimal hardware complexity. Furthermore, the power consumption can also be saved by using higher radix FFT algorithm.

2 ARCHITECTURAL OVERVIEW of FFT

Figure 1 highlights the basic memory-based continuous flow architecture where data streams are multiplexed between the processor I/O and the PE whose core computational unit is the mixed-radix FFT butterfly. As an example, I/O communicating to Memory Bank 1 will block communication between the FFT PE and Memory Bank 1. The FFT PE reads and writes to Memory Bank 2 instead. When Memory Bank 1 is full of new data, the FFT PE can begin reading and working on the data stored there. The I/O is then blocked from writing to Memory Bank 1 and must now write to Memory Bank 2.The FFT processing element thus alternates between memory banks, and as long as new data are sent to the non-active memory bank (i.e.,
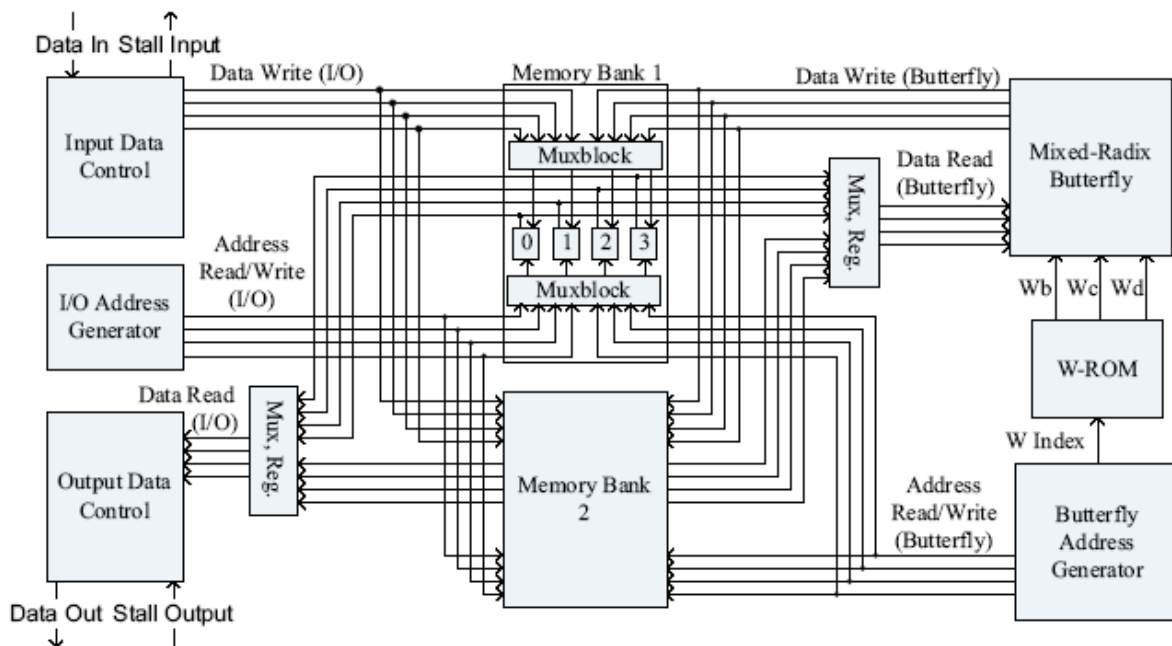


Fig. 1. FFT processor block diagram

the bank not being used by the PE), memory starvation is avoided and continuous operation of the PE occurs, maximizing the throughput of the FFT processor [16]. Notice that in order for the butterfly to read input data and write output data simultaneously, dual-port SRAMs are required. Similarly, the same argument can be said for the processor I/O. Continuous operation on a memory bank of only size $N$ necessitates that the address generation and control guarantee that no address conflicts occur during simultaneous read/writes. The in-place address generation scheme adopted by the processor is further described in Section III. For a radix-$r$ butterfly, we require $r$ memory subbanks to read and write data to and from the butterfly. As shown in Fig. 1, a radix-4 butterfly must read its four inputs $A$, $B$, $C$, and $D$ from the memory bank while writing to memory its four outputs: $U$, $V$, $X$, and $Y$. Our processor contains a single radix-4/-2 mixed-radix (MR) butterfly composed of three complex multipliers, 12 complex adders,

and rounding logic. The butterfly input and output utilizes 16-bit real and 16-bit imaginary data, for a combined 32-bit complex FFT word width. The processor calculates FFTs varying in size from 16- to 4096-point. Thus, for FFTs of length $N = 2r$ with $r$ even (i.e., integer powers of 4), the butterfly performs standard radix-4 computations throughout the entire FFT. For $r$ odd (i.e., $N = 32, 128, 512, 2048$) the butterfly functions as a radix-4 butterfly for the first $(r - 1)/2$ stages, and then switches mode to a radix-2 butterfly for the final stage. The base radix-4 butterfly can be easily turned into a radix-2 butterfly if we take the following two equations from Fig. 1,

$X = A - BW_b + CW_c - DW_d$ (1)

$Y = A + iBW_b - CW_c - iDW_d$ (2)

and set inputs $B$ and $D$ to zero [15].

In theory, radix-4 computations like those shown in Eq. 1 and Eq. 2 can grow larger than a factor of four due to the possibility of the input data having a range outside the unit circle on the real-imaginary complex plane. The butterfly by default only shifts the output data by two, but the user can chose to configure the butterfly to be conservative and shift the output data by four. This, however, causes a potential reduction in accuracy. Over the course of several
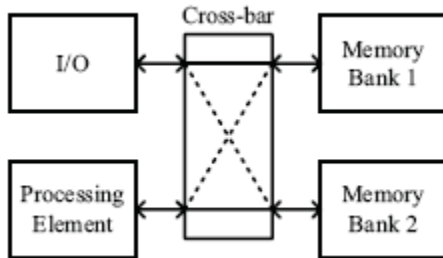
53

Fig.2. A continuous flow memory based FFT processor architecture

Fig. 2. A continuous flow memory based FFT processor architecture thousand simulations with random data, overflow has not occurred, so the possibility of overflow will likely appear only under degenerate cases. If overflow does occur while in the default shift-by-2 mode,the data are then saturated accordingly. The architecture also supports block floating point (BFP) tracking.Therefore, by grouping data to one "exponent," the maximum number of bits is preserved by shifting away the minimum number of redundant bits within that group of data. With BFP, the Signal to Quantization Noise Ratio (SQNR) of a 1024-point FFT can improve over 200%. Figure 2 shows the final architecture of our FFT processor, which is composed of an I/O subgroup and a FFT subgroup, both centered around two memory banks. The I/O subgroup mainly contains the I/O controllers. The FFT half consists of the address generator, twiddle factor ROM (W-ROM), and the MR butterfly. Each memory bank is composed of simple mux logic and four 1024-word SRAM modules.

## 3. MIMO OFDM

The growing demand of multimedia services and the growth of Internet related contents lead to increasing interest to high speed communications. The requirement for wide bandwidth and flexibility imposes the use of efficient transmission methods that would fit to the characteristics of wideband channels especially in wireless environment where the channel is very challenging. In wireless environment the signal is propagating from the transmitter to the

receiver along number of different paths, collectively referred as multipath. While propagating the signal power drops of due to three effects: path loss, macroscopic fading and microscopic fading. Fading of the signal can be mitigated

by different diversity techniques. To obtain diversity, the signal is transmitted through multiple (ideally) independent fading paths e.g. in time, frequency or space and combined constructively at the receiver. Multiple input- multiple-output (MIMO) exploits spatial diversity by having several transmit and receive antennas. However the paper "MIMO principles" assumed frequency flat fading MIMO channels. OFDM is modulation method known for its capability to mitigate multipath. In OFDM the high speed data

stream is divided into Nc narrowband data streams, Nc corresponding to the subcarriers or subchannels i.e. one OFDM symbol consists of N symbols modulated for example by QAM or PSK. As a result the symbol duration is N times longer than in a single carrier system with the same symbol rate. The symbol duration is made even longer by adding a cyclic prefix to each symbol. As long as the cyclic prefix is longer than the channel delay spread OFDM offers inter-symbol interference (ISI) free transmission. Another key advantage of OFDM is that it dramatically reduces equalization complexity by enabling equalization in the frequency domain. OFDM, implemented with IFFT at the transmitter and FFT at the receiver, converts the wideband signal, affected by frequency selective fading, into N narrowband flat fading signals [1] thus the equalization can be performed in the frequency domain by a scalar division carrier-wise with the subcarrier related

channel coefficients. The channel should be known or learned at the receiver. The combination MIMO-OFDM is very natural and beneficial since OFDM enables support of more antennas and larger bandwidths since it simplifies equalization dramatically in MIMO systems. MIMO-OFDM is under intensive investigation by researchers. This paper provides a general overview of this promising transmission technique.

The general transceiver structure of MIMO-OFDM is presented in Fig. 3. The system consists of N transmit antennas and M receive antennas. In this paper the cyclic prefix is

assumed to be longer than the channel delay spread. The OFDM signal for each antenna is obtained by using inverse fast Fourier transform (IFFT) and can be detected by fast Fourier transform (FFT). The received MIMO-OFDM symbol of the n:th subcarrier and the m:th OFDM symbol
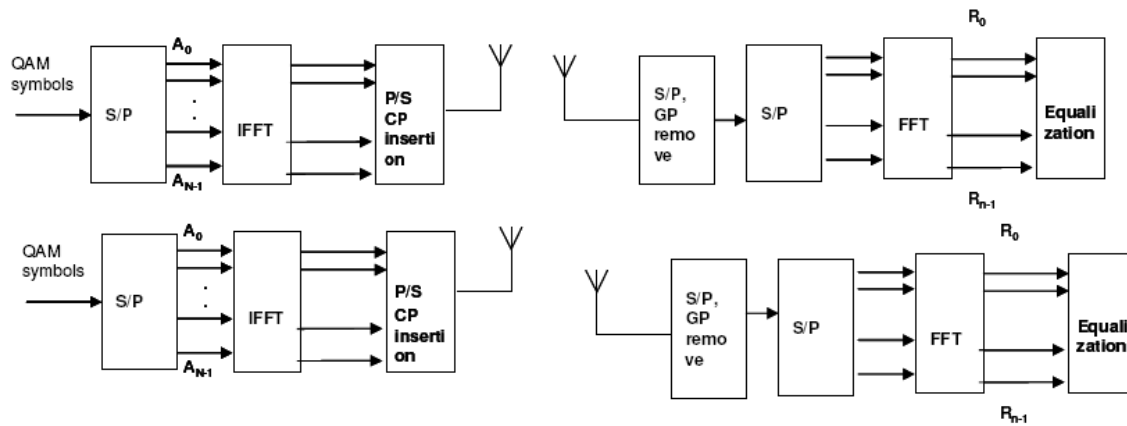


Fig 3  MIMO-OFDM transceiver

## 4. CONCLUSION

MIMO and MIMO-OFDM are very hot topics of current research. The information-theoretic performance limits, particularly in the multiuser context and space time code and receiver design have attracted significant research interest. OFDM is an effective technique to combat multi-path delay spread for wideband wireless transmission. OFDM with multiple transmit and receive antennas form a MIMO system to increase system capacity.

**Reference**

[1] A. Paulraj, R. Nabar, D. Gore: Introduction to Space-Time Wireless Communications, Published May 2003, ISBN: 0521826152
[2] V.D.Nguyen, M.Pätzhold, "Frequency domain interference cancellation for MIMO-OFDM systems" Proc. 9th International OFDM-Workshop,Dresden, Germany, 15. – 16. Sept. 2004, p. 114–117.

[3] P. Uthansaku M.E. Bialkows "Multipath signal effect on the capacity of MIMO, MIMO-OFDM and spread MIMO-OFDM" Microwaves, Radar and Wireless Communications, 2004. MIKON-2004. 15th International Conference on , Volume: 3 , 17-19 May 2004 Pages:989 - 992

[4] Y-L. Lee, Y-H. You, W-G. Jeon, J-H. Paik, H-K. Song, " Peak-to-average power ratio in MIMO-OFDM systems using selective mapping" IEE Communications letters, Vol. 7, No. 12, December 2003

[5] A.J. Paulraj, D.A. Gore, R.U. Nabar, H. Bölcskei, "An overview of MIMO communications - a key to gigabit wireless" Proceedings of the IEEE ,Volume: 92 , Issue: 2 , Feb. 2004 Pages:198 – 218


[1] Mujtaba *et al.*, TGn Sync Proposal Tech.Specification for IEEE 802.11 Task Group 2005, IEEE 802.11-04/0889r3.

[2] S. Magar, S. Shen, G. Luikuo, M. Fleming, and R. Aguilar, "An application specific DSP chip set for 100-MHz data rates,"in *Proc. Int. Conf. Acoustics, Speech, Signal Process.*, Apr. 1988, vol. 4, pp. 1989–1992.

[3] H. Shousheng and M. Torkelson, "Designing pipeline FFT processor for OFDM (de)modulation," in *Proc. URSI Int. Symp. on Signals, Syst, Electron.*, Oct. 1998, vol. 29, pp. 257–262.

[4] J. O'Brien, J. Mather, and B. Holland, "A 200 MIPS single-chip 1 k FFT processor," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1989, vol. 36, pp. 166–167,, 327.

[5] B. M. Bass, "A low-power, high-performance, 1024-point FFT processor," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 380–387, Mar. 1999.

[6] W.-C. Yeh and C.-W. Jen, "High-speed and low-power split-radix FFT," *IEEE Trans. Acoust.,Speech, Signal Process.*, vol. 51, no. 3, pp. 864–874, Mar. 2003.

57