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A BIST TPG for Low Power Dissipation and High Fault Coverage

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***Abstract*—This paper presents a low hardware overhead test pattern generator (TPG) for scan-based built-in self-test (BIST) that can reduce switching activity in circuits under test (CUTs) during BIST and also achieve very high fault coverage with reasonable lengths of test sequences. The proposed BIST TPG decreases transitions that occur at scan inputs during scan shift operations and hence reduces switching activity in the CUT. The proposed BIST is comprised of two TPGs: LT-RTPG and 3-weight WRBIST. Test patterns generated by the LT-RTPG detect easy-to-detect faults and test patterns generated by the 3-weight WRBIST detect faults that remain undetected after LT-RTPG patterns are applied. The proposed BIST TPG does not require modification of mission logics, which can lead to performance degradation. Experimental results for ISCAS'89 benchmark circuits demonstrate that the proposed BIST can significantly reduce switching activity during BIST while achieving 100% fault coverage for all ISCAS'89 benchmark circuits. Larger reduction in switching activity is achieved in large circuits. Experimental results also show that the proposed BIST can be implemented with low area overhead.**

***Index Terms*—Built-in self-test (BIST), heat dissipation during test application, low power testing, power dissipation during test application, random pattern testing.**

I. INTRODUCTION

Since in built-in self-test (BIST), test patterns are generated and applied to the circuit-under-test (CUT) by on-chip hardware, minimizing hardware overhead is a major concern of BIST implementation. Unlike stored pattern BIST, which requires high hardware overhead due to memory devices required to store precomputed test patterns, pseudorandom BIST, where test patterns are generated by pseudorandom pattern generators such as linear feedback shift registers (LFSRs) and cellular automata (CA), requires very little hardware overhead. However, achieving high fault coverage for CUTs that contain many random pattern resistant faults

(RPRFs) only with (pseudo) random patterns generated by an LFSR or CA often requires unacceptably long test sequences thereby resulting in prohibitively long test time. The random pattern test length required to achieve high fault coverage is often determined by only a few RPRFs [1].

Several techniques have been proposed to address this problem. Reseedable and/or reconfigurable LFSRs are proposed in [2]–[4]. In [5] and [6], random patterns that do not detect any new faults are mapped into deterministic tests for RPRFs. In test point insertion (TPI) techniques [7], [8], control and observation points are inserted at selected gates to improve detection probabilities of RPRFs. In weighted random pattern testing [1], [9]–[11], the outputs of test pattern generator (TPG) are biased to generate test sequences that have nonuniform signal probabilities to increase detection probabilities of RPRFs that escape pseudorandom test sequences, which have a uniform signal probability of 0.5. Random pattern generators proposed in [12] and [13] use Markov sources to exploit spatial correlation between state inputs that are consecutively located in the scan chain. A 3-weight weighted random BIST (3-weight WRBIST) can be classified as an extreme case of conventional weighted random pattern testing BIST. However, in contrast to conventional weighted random pattern testing BIST where various weights, e.g., 0, 0.25, 0.5, 0.75, 1.0, can be assigned to outputs of TPGs, in 3-weight WRBIST, only three weights, 0, 0.5, and 1, are assigned. Since only three weights are used, circuitry to generate weights is simple; weight 1 (0) is obtained by fixing a signal to a 1 (0) and weight 0.5 by driving a signal by an output of a pseudorandom pattern generator, such as an LFSR. Weight sets are calculated from test cubes for RPRFs.

II. 3-WEIGHT WRBIST

A. Generator

In this paper, we assume that the sequential CUT has m primary and state inputs, and employs full-scan. Even though the proposed BIST TPG is applicable to scan designs with multiple scan chains, we assume that all m primary and state inputs are driven by a single scan chain unless stated otherwise (application to multiple scan chains is discussed separately in Section V) only for clarity and convenience of illustration. A *test cube* is a test pattern that has unspecified inputs. The *detection probability* of a fault is defined as the probability that a randomly generated test pattern detects the fault [1]. In the 3-weight WRBIST scheme, fault coverage for a random pattern resistant circuit is enhanced by improving detection probabilities of RPRFs; the detection probability of an RPRF is improved by fixing some inputs of the CUT to the values specified in a deterministic test cube for the RPRF. A *generator* or *weight set* is a vector that represents weights that are assigned to inputs of the circuit during 3-weight

WRBIST. Inputs that are assigned weight 1 (0) are fixed to 1 (0) and inputs that are assigned weight 0.5 are driven by outputs of the pseudorandom pattern generator, such as an LFSR and a CA. A generator is calculated from a set of deterministic test cubes for RPRFs.

Inputs that are assigned

U's in a generator are called *conflicting inputs* of the generator.

C	$p_5\ p_4\ p_3\ p_2\ p_1 p_0$	F	dp
c^0	1 X 1 1 X 0	f^0	$1/2^4$
c^1	X 0 1 0 0 X	f^1	$1/2^4$
c^2	1 X X 0 X 1	f^2	$1/2^3$
c^3	0 0 X 0 0 1	f^3	$1/2^5$
$gen(C)$	U 0 1 U 0 U		

(a)

C^0	$p_5 p_4 p_3 p_2 p_1 p_0$
c^0	1 X 1 1 X 0
c^1	X 0 1 0 0 X
$gen(C^0)$	1 0 1 U 0 0

C^1	$p_5 p_4 p_3 p_2 p_1 p_0$
c^2	1 X X 0 X 1
c^3	0 0 X 0 0 1
$gen(C^1)$	U 0 X 0 0 1

(b)

Fig. 1. Example test cube sets. (a) Testcube set . (b) Testcube subsets .

(weight sets).

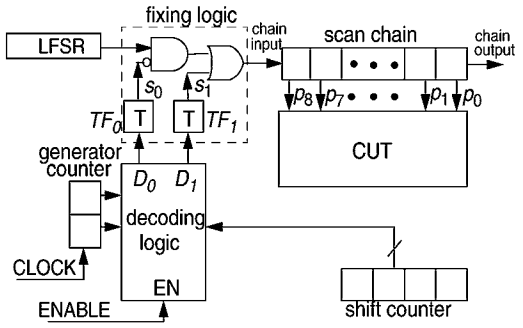
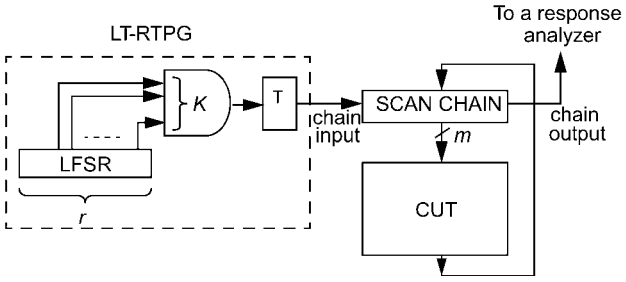


Fig. 2. Exemplary 3-weight WRBIST.

A. LT-RTPG

The LT-RTPG proposed in [23] reduces switching activity during BIST by reducing transitions at scan inputs during scan shift operations. An example LT-RTPG is shown in Fig. 3. The LT-RTPG is comprised of an r -stage LFSR,

Fig.3. LT-RTPG.



K -input AND gate, and a toggle flip-flop (T flip-flop). Hence, it can be implemented with very little hardware. Each of

K inputs of the AND gate is connected to either a normal or an inverting output of the

r LFSR stages. If large

K is used, large sets of neighboring state inputs will be assigned identical values in most test patterns, resulting in the decrease fault coverage or the increase in test sequence length. Hence, like [23], in this paper, LT-RTPGs with only

$K = 2$ or 3 are used. Since a

T flip-flop holds previous values until the input of the

T flip-flop is assigned a 1, the same value

v, where

$v \in \{0,1\}$, is repeatedly scanned into the scan chain until the value at the output of the AND gate becomes 1. Hence, adjacent scan flip-flops are assigned identical values in most test patterns and scan inputs have fewer transitions during scan shift operations. Since most switching activity during scan BIST occurs during scan shift operations (a capture cycle occurs at every

$m+1$ cycles), the LT-RTPG can reduce heat dissipation during overall scan testing. Various properties of the LT-RTPG are studied and a detailed methodology for its design is presented in [23].

It has been observed that many faults that escape random patterns are highly correlated with each other and can be detected by continuously complementing values of a few inputs from a parent test vector. This observation is exploited in [26][27], [31], and [32] to improve fault coverage for circuits that have large numbers of RPRFs. We have also observed that tests for faults that escape LT-RTPG test sequences share many common input assignments. This implies that RPRFs that escape LT-RTPG test sequences can be effectively detected by fixing selected inputs to binary values specified in deterministic test cubes for these RPRFs and applying random patterns to the rest of inputs. This technique is used in the 3-weight WRBIST to achieve high fault coverage for random pattern resistant circuits. In this paper we demonstrate that augmenting the LT-RTPG with the serialfixing 3-weight WRBIST proposed in [27] can attain high fault coverage without excessive switching activity or large area overhead even for circuits that have large numbers of RPRFs.

VI. Experimental Results

Table I compares results obtained by applying test sequences generated by regular LFSRs (*LFSR sequences*, for short) and results obtained by applying test sequences generated by the proposed TPGs (*the proposed TPG sequences*, for short). Columns under the heading *LFSR* give results of LFSR sequences while columns under the heading *proposed* give results of proposed TPG sequences. The column # *pat* under the heading LFSR shows the number of test patterns generated by the LFSR and the column achieved

TABLE I Comparisons With LFSR Generated Patterns (Single Scan Chain)

	LFSR			*Proposed*														
					K = 2							*K = 3*						
CKT Name	*# pat*	*stuck at FE %*	*# Aver. Trans.*	*# LT-RTG pat*	*LT-RTG FE%*	*# gen*	*tot. # pat.*	*Switching LT-RTG*	*SW-TPG*	*Trans dly FE%*	*run time (sec)*	*LT-RTG FE%*	*# gen*	*tot. # pat.*	*Switching LT-RTG*	*SW-TPG*	*Trans dly FE%*	*run time (sec)*
s1423	4096	99.08	339	2048	97.94	2	2904	.64	.72	99.75	4	96.04	4	2560	.45	.76	99.75	4
s5378	32768	99.75	1221	16384	96.13	4	20480	.73	.59	99.77	4	93.68	7	23552	.58	.69	99.50	5
s9234	132072	95.56	2717	16384	86.14	15	31744	.61	.49	99.55	627	82.35	18	34816	.38	.51	99.59	280
s13207	132072	99.76	4585	16384	89.27	9	25600	.73	.43	99.97	37	84.40	11	27648	.55	.41	99.91	83
s15850	528288	97.63	4773	16384	93.49	9	25600	.65	.54	99.72	165	90.79	14	30720	.44	.47	99.72	182
s38417	528288	99.31	12476	65536	93.86	29	124928	.67	.47	99.82	1399	93.65	31	129024	.44	.41	99.92	1557
s38584	528288	99.18	11211	32768	93.51	9	51200	.64	.45	99.96	601	91.49	16	65536	.41	.54	99.96	772
average	269410	98.61			92.91		40265	.67	.53	99.79		90.34		44837	.46	.54	99.76	

by the LFSR sequence.

VII. CONCLUSION

This paper presents a low hardware overhead TPG for scan-based BIST that can reduce switching activity in CUTs during BIST and also achieve very high fault coverage with a reasonable length of test sequence. Unacceptably long test sequences are often required to attain high fault coverage with pseudorandom test patterns for circuits that have many random pattern resistant faults. The main objective of most recent BIST techniques has been the design of TPGs that achieve high fault coverage at acceptable test lengths for such circuits. While this objective still remains important, reducing heat dissipation during test application is also becoming an important objective. Since the correlation between consecutive patterns applied to a circuit during BIST is significantly lower, switching activity in the circuit can be significantly higher during BIST than that during its normal operation. Excessive switching activity during test application can cause several problems. The proposed TPG reduces the number of transitions that occur at scan inputs during scan shifting by scanning in the test patterns where neighboring bits are highly correlated. The proposed BIST is comprised of two TPGs: LT-RTPG [23] and 3-weight WRBIST [27]. Test sequences generated by the LT-RTPG detect easy-to-detect faults. Faults that escape LT-RTPG test sequences are detected by test patterns generated by the 3-weight WRBIST. The number of weight sets (generators) is minimized by guiding the proposed ATPG with cost functions that reflect the number of conflicting inputs to be incurred by setting an input to a binary value. An algorithm to design the 3-weight WRBIST that requires minimal hardware overhead and whose patterns cause minimal number of transitions during scan shift cycles is presented. Hardware overhead for the proposed TPG is further reduced by identifying compatible scan chains in multiple scan chain designs. Experimental results for ISCAS'89 benchmark circuits demonstrate that the proposed BIST can significantly reduce switching activity during BIST while achieving 100% fault coverage for all benchmark circuits. Larger reduction in switching activity is achieved for large circuits, which have long scan chains. The proposed BIST structure does not require modification of mission logic which can cause performance degradation. Experimental results for large industrial circuits demonstrate that the proposed TPG can significantly improve fault coverage of LFSR generated test sequences with low hardware overhead.

REFERENCES

[1] P. H. Bardell, W. H. McAnney, and J. Savir, *Built-In Test for VLSI: Pseudorandom Techniques*. New York: Wiley, 1987.

[2] S. Hellebrand, J. Rajski, S. Tarnick, S. Venkataraman, and B. Courtois, "Built-In test for circuits with scan based on reseeding of multiple-polynomial linear feedback shift registers," *IEEE Trans. Comput.*, vol. 44, no. 2, pp. 223–233, Feb. 1995.

[3] N. Zacharia, J. Rajski, and J. Tyszer, "Decompression of test data using variable-length seed LFSRs," in *Proc. IEEE 13th VLSI Test Symp.*, 1995, pp. 426–433.

[4] S. Hellebrand, S. Tarnick, and J. Rajski, "Generation of vector patterns through reseeding of multiple-polynomial linear feedback shift registers," in *Proc. IEEE Int. Test Conf.*, 1992, pp. 120–129.

[5] N. A. Touba and E. J. McCluskey, "Altering a pseudo-random bit sequence for scan-based BIST," in *Proc. IEEE Int. Test Conf.*, 1996, pp. 167–175.

[6] M. Chatterjee and D. K. Pradhan, "A new pattern biasing technique for BIST," in *Proc. VLSITS*, 1995, pp. 417–425.

[7] N. Tamarapalli and J. Rajski, "Constructive multi-phase test point insertion for scan-based BIST," in *Proc. IEEE Int. Test Conf.*, 1996, pp. 649–658.

[8] Y. Savaria, B. Lague, and B. Kaminska, "A pragmatic approach to the design of self-testing circuits," in *Proc. IEEE Int. Test Conf.*, 1989, pp. 745–754.

[9] J. Hartmann and G. Kemnitz, "How to do weighted random testing for BIST," in *Proc. IEEE Int. Conf. Comput.-Aided Design*, 1993, pp. 568–571.

[10] J. Waicukauski, E. Lindbloom, E. Eichelberger, and O. Forlenza, "A method for generating weighted random test patterns," *IEEE Trans. Comput.*, vol. 33, no. 2, pp. 149–161, Mar. 1989.

[11] H.-C. Tsai, K.-T. Cheng, C.-J. Lin, and S. Bhawmik, "Efficient test-point selection for scan-based BIST," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 6, no. 4, pp. 667–676, Dec. 1998.

[12] W. Li, C. Yu, S. M. Reddy, and I. Pomeranz, "A scan BIST generation method using a markov source and partial BIST bit-fixing," in *Proc. IEEE-ACM Design Autom. Conf.*, 2003, pp. 554–559.

[13] N. Z. Basturkmen, S. M. Reddy, and I. Pomeranz, "Pseudo random patterns using markov sources for scan BIST," in *Proc. IEEE Int. Test Conf.*, 2002, pp. 1013–1021.

[14] Y. Zorian, "A distributed BIST control scheme for complex VLSI devices," in *Proc. VLSI Testing Symp.*, 1993, pp. 4–9.

[15] S. W. Golomb, *Shift Register Sequences*. Laguna Hills, CA: Aegean Park, 1982.

[16] C.-Y. Tsui, M. Pedram, C.-A. Chen, and A. M. Despain, "Low power state assignment targeting two-and multi-level logic implementation," in *Proc. IEEE Int. Conf. Comput.-Aided Des.*, 1994, pp. 82–87.

[17] P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, "A test vector inhibiting technique for low energy BIST design," in *Proc. VLSI Test. Symp.*, 1999, pp. 407–412.

[18] V. Dabholkar, S. Chakravarty, I. Pomeranz, and S. Reddy, "Techniques for minimizing power dissipation in scan and combinational circuits during test application," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 17, no. 12, pp. 1325–1333, Dec. 1998.

[19] R. M. Chou, K. K. Saluja, and V. D. Agrawal, "Scheduling tests for VLSI systems under power constraints," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 5, no. 2, pp. 175–185, Jun. 1997.

[20] T. Schuele and A. P. Stroele, "Test scheduling for minimal energy con-

sumption under power constrainits," in *Proc. VLSI Test. Symp.*, 2001, pp. 312–318.

[21] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective*, 2nd ed. Reading, MA: Addison-Wesley, 1992.

[22] S. Gerstendorfer and H.-J. Wunderlich, "Minimized power consumption for scan-based BIST," in *Proc. IEEE Int. Test Conf.*, 1999, pp. 77–84.

[23] S. Wang and S. K. Gupta, "LT-RTPG: A new test-per-scan BIST TPG for low heat dissipation," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 25, no. 8, pp. 1565–1574, Aug. 2006.

[24] S. Wang and S. K. Gupta, "DS-LFSR: A BIST TPG for low heat dissipation," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 21, no. 7, pp. 842–851, Jul. 2002.

[25] F. Corno, M. Rebaudengo, M. S. Reorda, G. Squillero, and M. Violante, "Low power BIST via non-linear hybrid celluar automata," in *Proc. VLSI Test. Symp.*, 2000, pp. 29–34.

[26] S. Wang, "Generation of low power dissipation and high fault coverage patterns for scan-basedBIST," in *Proc. IEEE Int. Test Conf.*, 2002, pp. 834–843.

[27] S. Wang, "Low hardware overhead scan based 3-weight weighted random BIST," in *Proc. IEEE Int. Test Conf.*, 2001, pp. 868–877.

[28] S. Wang, "Minimizing Heat Dissipation During Test Application," Ph.D. dissertation, EE-Systems Dept., Univ. Southern California, Los Angeles, 1998.

[29] L. H. Goldstein and E. L. Thigpen, "SCOAP: Sandia controllability/observability analysis program," in *Proc. IEEE-ACM Des. Autom. Conf.*, 1980, pp. 190–196.

[30] P. Goel, "An implicit enumeration algorithm to generate tests for combinational logic circuits," *IEEE Trans. Comput.*, vol. C-30, no. 3, pp. 215–222, Mar. 1981.

[31] K.-H. Tsai, J. Rajski, and M. Marek-Sadowska, "Star test: The theory and its applications," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 19, no. 9, pp. 1052–1064, Sep. 2000.

[32] I. Pomeranz and S. Reddy, "3-weight pseudo-random test generation based on a deterministic test set for combinational and sequential circuits," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 12, pp. 1050–1058, Jul. 1993.

[33] T. H. Cormen, C. E. Leiserson, and R. L. Rivest, *Introduction to Algorithm*. Cambirdge, MA: MIT Press, 1990.

[34] J. Savir, "Skewed-load transition test: Part I, calculus," in *Proc. IEEE Int. Test Conf.*, 1992, pp. 705–713.

[35] E. M. Sentovich, K. J. Singh, L. Lavagno, C. Moon, R. Murgai, A. Saklanha, H. Savoj, P. R. Stephan, R. K. Brayton, and A. Sangiovanni-Vincentelli, "SIS: A system for sequential circuit synthesis," Electron. Res. Lab. Memorandum, Univ. California, Los Angeles, UCB/ERL M92/41, 1992.

[36] L. Li and K. Chakrabarty, "Test set embedding for deterministic BIST using a reconfigurable interconnect network," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 23, no. 9, pp. 1289–1305, Sep. 2004.

[37] N.-C. Lai, S.-J. Wang, and Y.-H. Fu, "Low-power BIST with a smoother and scan-chain reorder under optimal cluster size," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 25, no. 11, pp. 2586–2594, Nov. 2006.

[38] N. Z. Basturkmen, S. M. Reddy, and I. Pomeranz, "A low power pseudo-random BIST technique," *J. Electron. Test.: Theory Appl.*, vol. 19, no. 6, pp. 637–644, Dec. 2003.